

High Reliability CMOS Programmable Universal Asynchronous Receiver/Transmitter (UART)

March 1997

Features

- · Two Operating Modes
 - Mode 0 Functionally Compatible with Industry Types Such as the TR1602A and CDP6402
 - Mode 1 Interfaces Directly with CDP1800 Series Microprocessors without Additional Components
- · Full or Half-Duplex Operation
- · Parity, Framing, and Overrun Error Detection
- Fully Programmable with Externally Selectable Word Length (5-8 Bits), Parity Inhibit, Even/Odd Parity, and 1, 1-1/2, or 2 Stop Bits

Ordering Information

PACK-	TEMP.	5V/200K	10V/400K	PKG.
AGE	RANGE	BAUD	BAUD	NO.
SBDIP	-55°C to +125°C	CDP1854ACD3	CDP1854ACD3	D40.6

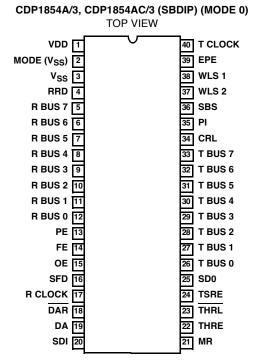
Description

The CDP1854A/3 and CDP1854AC/3 are high reliability silicon gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A/3 is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

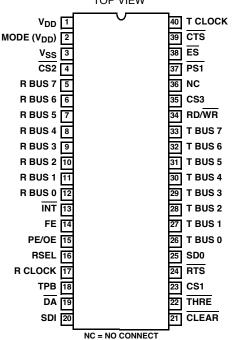
The CDP1854A/3 UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE = 1), the CDP1854A/3 is directly compatible with the CDP1800 series microprocessor system without additional interface circuitry. When the mode input is low (MODE = 0), the device is functionally compatible with industry standard UARTs such as the TR1602A and CDP6402. It is also pin compatible with these types, except that pin 2 is used for the mode control input.

The CDP1854A/3 and the CDP1854AC/3 are functionally identical. The CDP1854A/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1854AC/3 has a recommended operating voltage range of 4V to 6.5V.

Pinouts



CDP1854A/3, CDP1854AC/3 (SBDIP) (MODE 1) TOP VIEW



Absolute Maximum Ratings

DC Supply-Voltage Range, (V _{DD}) (All voltages referenced to V _{SS} terminal)
CDP1854A/30.5 to +11V
CDP1854AC/30.5 to +7V
Input Voltage Range, All Inputs0.5 to V _{DD} +0.5V
DC Input Current, Any One Input±10mA
Device Dissipation Per Output Transistor
For T _A = Full Package-Temperature Range 100mW
Operating-Temperature Range (T _A)
Package Type D -55 ⁰ C to ±125 ⁰ C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ _{JA} (^o C/W)	θ_{JC} ($^{o}C/W$)
SBDIP Package	55	15
Maximum Junction Temperature		+150 ⁰ C
Maximum Storage Temperature Range (T	- STG)65 ⁰	'C to +150°C
Maximum Lead Temperature (Soldering 1	0s)	
At Distance 1/16 ±1/32 inch (1.59 ±0.79	9mm)	+265 ⁰ C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Static Electrical Specifications

		CONDITIONS				LIMITS				
		V-	V _{IN}	V	-55 ⁰ C,	+25°C	+125°C			
PARAMETER		ν _Ο (V)	(V)	V _{DD} (V)	MIN	MAX	MIN	MAX	UNITS	
Quiescent Device Current	I _{DD}	-	0, 5	5	-	500	-	1000	μΑ	
		-	0, 10	10	-	500	-	1000	μΑ	
Output Low Drive	l _{OL}	0.4	0, 5	5	0.75	-	0.5	-	mA	
(Sink) Current		0.5	0, 10	10	1.80	-	1.2	-	mA	
Output High Drive	I _{OH}	4.6	0, 5	5	-	-0.5	-	-0.35	mA	
(Source) Current	9.5	0, 10	10	-	-1.0	=	-0.70	mA		
Output Voltage Low-Level	V _{OL}	-	0, 5	5	-	0.1	-	0.2	V	
(Note 1)		-	0, 10	10	-	0.1	-	0.2	V	
Output Voltage High Level (Note 1)	V _{OH}	-	0, 5	5	4.9	-	4.9	-	V	
High Level (Note 1)		-	0, 10	10	9.9	-	9.8	-	V	
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	=	1.5	V	
		0.5, 9.5	-	10	-	3	=	3	V	
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V	
		0.5, 9.5	-	10	7	-	7	-	V	
Input Leakage Current	I _{IN}	-	0, 5	5	-	±1	-	±5	μΑ	
		-	0, 10	10	-	±1	-	±5	μΑ	
Three-State Output	lout	0, 5	0, 5	5	-	±1	-	±10	μΑ	
Leakage Current		0, 10	0, 10	10	-	±1	-	±10	μΑ	
Input Capacitance (Note 1)	C _{IN}	-	-	-	-	10	-	10	pF	
Output Capacitance (Note 1)	C _{OUT}	-	-	-	-	15	-	15	pF	

NOTE:

1. Guaranteed but not tested.

Specifications CDP1854A/3, CDP1854AC/3

Operating Conditions At T_A = Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

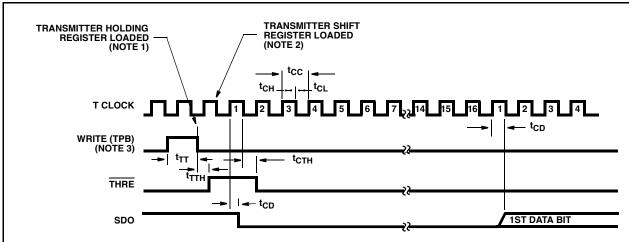
	CONDITIONS LIMITS					
	V	-55 ^o C,	+25°C	+12	5°C	
PARAMETER	V _{DD} (V)	MIN	MAX	MIN	MAX	UNITS
DC Operating Voltage Range	=	4	10.5	4	6.5	٧
Input Voltage Range	-	V _{SS}	V_{DD}	V _{SS}	V_{DD}	٧
Baud Rate (Receive or Transmit)	5	-	250	-	215	K bits/s
	10	-	520	-	430	K bits/s

Dynamic Electrical Specifications t_{R} , t_{F} = 15ns, V_{IH} = V_{DD} , V_{IL} = V_{SS} , C_{L} = 100pF, (See Figure 1)

		.,	-55 ^o C,	-55°C, +25°C		5°C	
PARAMETER		V _{DD} (V)	MIN	MAX	MIN	MAX	UNITS
TRANSMITTER TIMING - MODE 1							
Clock Period	t _{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width	t _{CL}						
Clock Low Level		5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	t _{CH}	5	135	-	155	-	ns
		10	65	-	80	-	ns
ТРВ	t _{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Propagation Delay Time	t _{CD}						
Clock to Data Start Bit		5	-	425	-	485	ns
		10	-	205	-	235	ns
TPB to THRE	t _{TTH}	5	-	315	-	380	ns
		10	-	155	-	185	ns
Clock to THRE	tстн	5	-	335	-	390	ns
		10	-	160	-	190	ns

$\textbf{Dynamic Electrical Specifications} \ \ t_{R}, t_{F} = 15 \text{ns}, \ V_{IH} = V_{DD}, \ V_{IL} = V_{SS}, \ C_{L} = 100 \text{pF}, \ (\text{See Figure 2})$

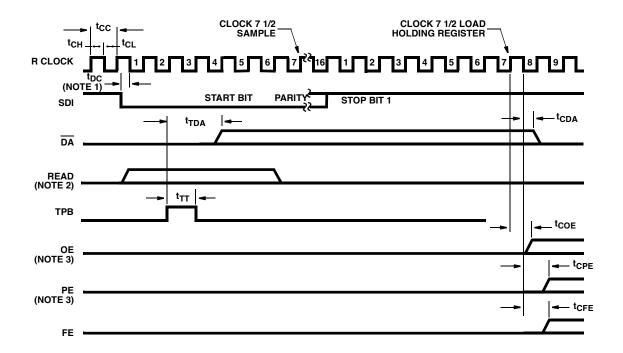
		.,	-55°C, +25°C		+125 ^o C		
PARAMETER		V _{DD} (V)	MIN	MAX	MIN	MAX	UNITS
RECEIVER TIMING - MODE 1			•	•			
Clock Period	t _{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width							
Clock Low Level	t _{CL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	^t CH	5	135	-	155	-	ns
		10	65	-	80	-	ns
ТРВ	t _{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Setup Time							
Data Start Bit to Clock	t_{DC}	5	105	-	120	-	ns
		10	65	-	70	-	ns
Propagation Delay Time							
TPB to DATA AVAILABLE	t _{TDA}	5	-	295	-	340	ns
		10	-	150	-	170	ns
Clock to DATA AVAILABLE	t _{CDA}	5	-	305	-	355	ns
		10	-	150	-	170	ns
Clock to Overrun Error	t _{COE}	5	-	305	-	330	ns
		10	-	150	-	175	ns
Clock to Parity Error	t _{CPE}	5	-	305	-	330	ns
		10	-	150	-	175	ns
Clock to Framing Error	t _{CFE}	5	-	280	-	330	ns
		10	-	145	-	165	ns



NOTES:

- 1. The holding register is loaded on the trailing edge of TPB.
- 2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{TC} after the trailing edge of TPB and transmission of a start bit occurs 1/2 clock period + t_{CD} later.
- 3. Write is the overlap of TPB, CS1, and CS3 = 1 and $\overline{\text{CS3}}$, RD/ $\overline{\text{WR}}$ = 0

FIGURE 1. TRANSMITTER TIMING DIAGRAM - MODE 1



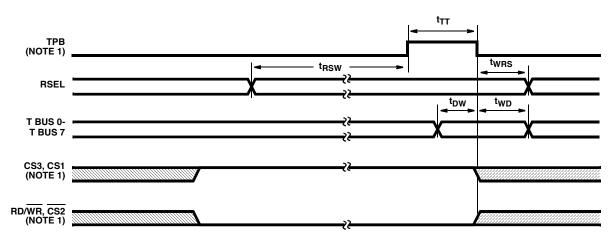
NOTES:

- 1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
- 2. Read is the overlap of CS1, CS3, RD/WR = 1 and CS2 = 0. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.
- 3. OE and PE share terminal 15 and are also available as two separate bits in the status register.

FIGURE 2. MODE 1 RECEIVER TIMING DIAGRAM

 $\textbf{Dynamic Electrical Specifications} \ \ t_{R}, t_{F} = 15 \text{ns}, \ V_{IH} = V_{DD}, \ V_{IL} = V_{SS}, \ C_{L} = 100 \text{pF}, \ (\text{See Figure 3})$

				LIM	IITS		
		V	-55 ⁰ C,	+25°C	+12	5°C	
PARAMETER		V _{DD} (V)	MIN	MAX	MIN	MAX	UNITS
CPU INTERFACE - WRITE TIMING - M	ODE 1						
Pulse Width							
ТРВ	t _{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Setup Time							
RSEL to Write	t _{RSW}	5	20	-	10	-	ns
		10	25	-	25	-	ns
Data to Write	t _{DW}	5	65	-	75	-	ns
		10	45	-	50	-	ns
Hold Time							
RSEL after Write	t _{WRS}	5	-10	-	-20	-	ns
		10	5	-	5	-	ns
Data after Write	t _{WD}	5	95	-	105	-	ns
		10	55	-	55	-	ns



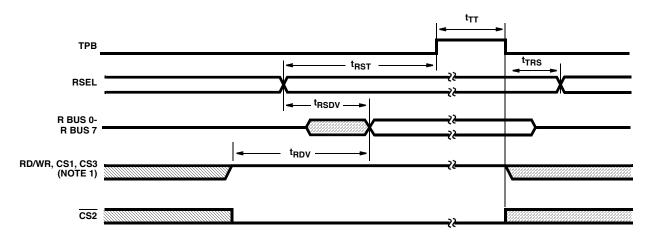
NOTE:

1. Write is the overlap of TPB, CS1, CS3 = 1 and $\overline{\text{CS2}}$, RD/ $\overline{\text{WR}}$ = 0.

FIGURE 3. MODE 1 CPU INTERFACE (WRITE) TIMING DIAGRAM

 $\textbf{Dynamic Electrical Specifications} \ \ t_{R}, t_{F} = 15 \text{ns}, \ V_{IH} = V_{DD}, \ V_{IL} = V_{SS}, \ C_{L} = 100 \text{pF}, \ (\text{See Figure 4})$

				LIMITS			
		V	-55 ⁰ C,	+25°C	+12	5°C	
PARAMETER		V _{DD} (V)	MIN	MAX	MIN	MAX	UNITS
CPU INTERFACE - READ TIMING - MO	DE 1						
Pulse Width							
ТРВ	t _{TT}	5	125	-	165	-	ns
		10	70	-	80	-	ns
Setup Time							
RSEL to TPB	t _{RST}	5	15	-	0	-	ns
		10	20	-	10	-	ns
Hold Time							
RSEL after TPB	t _{TRS}	5	-10	-	-25	-	ns
		10	5	-	0	-	ns
Propagation Delay Time							
Read to Data Valid Time	t_{RDV}	5	-	360	-	420	ns
		10	-	165	-	195	ns
RESEL to Data Valid Time	t _{RSDV}	5	-	250	-	295	ns
		10	-	125	-	145	ns



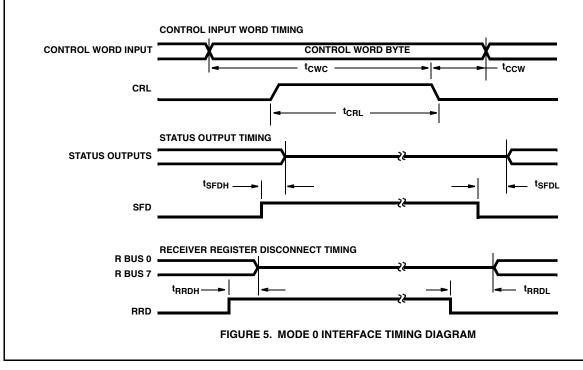
NOTE:

1. Read is the overlap of CS1, CS3, RD/ \overline{WR} = 1 and $\overline{CS2}$ = 0.

FIGURE 4. MODE 1 CPU INTERFACE (READ) TIMING DIAGRAM

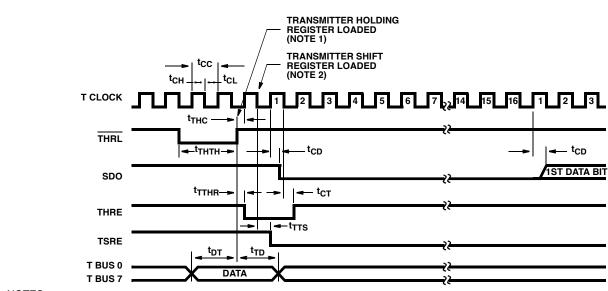
 $\textbf{Dynamic Electrical Specifications} \ \ t_{R}, t_{F} = 15 \text{ns}, \ V_{IH} = V_{DD}, \ V_{IL} = V_{SS}, \ C_{L} = 100 \text{pF}, \ (\text{See Figure 5})$

				LIM	IITS		
		V _{DD}	-55°C, +25°C		+125°C		
PARAMETER		(V)	MIN	MAX	MIN	MAX	UNITS
INTERFACE TIMING - MODE 0							
Pulse Width							
CRL	t _{CRL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
MR	t _{MR}	5	340	-	385	-	ns
		10	160	-	175	=	ns
Setup Time							
Control Word to CRL	t _{CWC}	5	80	-	85	-	ns
		10	40	-	60	-	ns
Hold Time							
Control Word after CRL	tCCW	5	65	-	65	-	ns
		10	45	-	45	-	ns
Propagation Delay Time							
SFD High to SOD	^t SFDH	5	-	175	-	195	ns
		10	-	105	-	115	ns
SFD Low to SOD	tSFDL	5	165	-	195	-	ns
		10	90	-	105	=	ns
RRD High to Receiver Register	t _{RRDH}	5	-	185	-	205	ns
High Impedance		10	-	110	-	130	ns
RRD Low to Receiver Register Active	tRRDL	5	165	-	195	-	ns
		10	90	-	105	-	ns



Dynamic Electrical Specifications t_{R} , t_{F} = 15ns, V_{IH} = V_{DD} , V_{IL} = V_{SS} , C_{L} = 100pF, (See Figure 6)

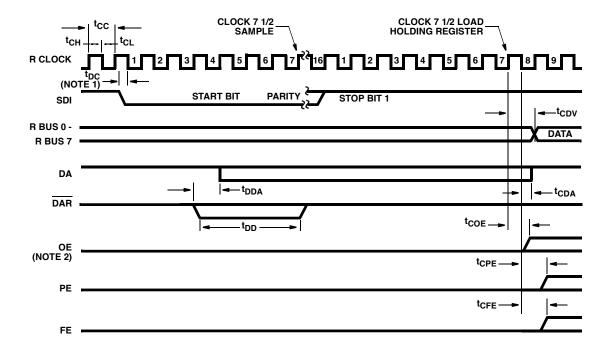
		V_{DD}	-55 ⁰ C	, +25 ^o C	+12	25°C	
PARAMETER		(V)	MIN	MAX	MIN	MAX	UNITS
TRANSMITTER TIMING - MODE 0	•						
Clock Period	t _{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width							
Clock Low Level	t _{CL}	5	105	-	125	-	ns
		10	55	-	65	-	ns
Clock High Level	t _{CH}	5	135	-	155	-	ns
		10	65	-	80	-	ns
THRL	t _{THTH}	5	140	-	165	-	ns
	Ī	10	80	-	85	-	ns
Setup Time							
THRL to Clock	t _{THC}	5	205	-	235	-	ns
		10	120	-	140	-	ns
Data to THRL	t _{DT}	5	25	-	30	-	ns
		10	20	-	25	-	ns
Hold Time							
Data after THRL	t_{TD}	5	60	-	95	-	ns
		10	45	-	75	-	ns
Propagation Delay Time							
Clock to Data Start Bit	t _{CD}	5	-	435	-	505	ns
		10	-	205	-	235	ns
Clock to THRE	t _{CT}	5	-	345	-	420	ns
		10	-	175	-	200	ns
THRL to THRE	t _{TTHR}	5	-	275	-	325	ns
	Ī	10	-	145	-	165	ns
Clock to TSRE	t _{TTS}	5	-	345	-	405	ns
	ļ	10	-	165	-	190	ns



NOTES:

- 1. The holding register is loaded on the trailing edge of THRL.
- 2. The transmitter shift register, if empty, is loaded on the first high-to-low transition of the clock which occurs at least 1/2 clock period + t_{THC} after the trailing edge of THRL and transmission of a start bit occurs 1/2 clock period + t_{CD} later.

FIGURE 6. MODE 0 TRANSMITTER TIMING DIAGRAM



NOTES:

- 1. If a start bit occurs at a time less than t_{DC} before a high-to-low transition of the clock, the start bit may not be recognized until the next high-to-low transition of the clock. The start bit may be completely asynchronous with the clock.
- 2. If a pending DA has not been cleared by a read of the receiver holding register by the time a new word is loaded into the receiver holding register, the OE signal will come true.

FIGURE 7. MODE 0 RECEIVER TIMING DIAGRAM

$\textbf{Dynamic Electrical Specifications} \ \, t_{R},\, t_{F} = 15 \text{ns},\, V_{IH} = V_{DD},\, V_{IL} = V_{SS},\, C_{L} = 100 \text{pF},\, (\text{See Figure 7})$

				LIM	IITS		
		V_{DD}	-55 ⁰ C	, +25 ^o C	+12	25°C	
PARAMETER		(V)	MIN	MAX	MIN	MAX	UNITS
RECEIVER TIMING - MODE 0				_	_		
Clock Period	t _{CC}	5	240	-	280	-	ns
		10	120	-	145	-	ns
Pulse Width							
Clock Low Level	^t CL	5	105	-	125	-	ns
		10	55	-	65	=	ns
Clock High Level	^t CH	5	135	-	155	-	ns
		10	65	-	80	-	ns
DATA AVAILABLE RESET	t _{DD}	5	75	-	90	=	ns
	•	10	45	-	50	-	ns
Setup Time							
Data Start Bit to Clock	t_{DC}	5	105	-	130	=	ns
		10	65	-	85	-	ns
Propagation Delay Time							
DATA AVAILABLE RESET to Data Available	t _{DDA}	5	-	240	-	280	ns
Data Available		10	-	130	-	145	ns
Clock to Data Valid	t _{CDV}	5	-	360	-	420	ns
		10	-	175	-	195	ns
Clock to Data Available	t _{CDA}	5	-	320	-	375	ns
		10	-	155	-	180	ns
Clock to Overrun Error	tCOE	5	-	365	-	415	ns
		10	-	170	-	190	ns
Clock to Parity Error	t _{CPE}	5	-	275	-	320	ns
		10	-	135	-	155	ns
Clock to Framing Error	t _{CFE}	5	-	270	-	320	ns
	ŀ	10	-	135	-	165	ns

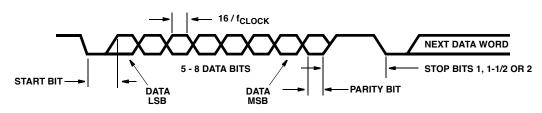
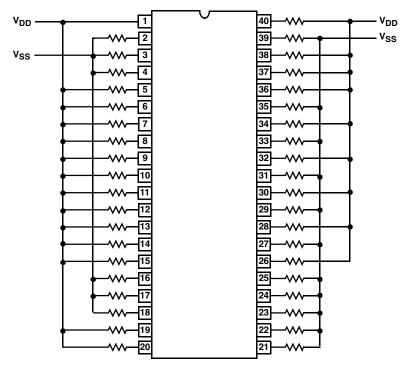


FIGURE 8. SERIAL DATA WORD FORMAT

Burn-In Circuit



ALL RESISTORS ARE 47k Ω ±20%

TYPE	V_{DD}	TEMPERATURE	TIME
CDP1854A/3	11	+125 ^o C	160 hrs.
CDP1854AC/3	7	+125 ^o C	160 hrs.

FIGURE 9. BIAS/STATIC BURN-IN CIRCUIT

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