



D8259

Programmable Interrupt Controller

ver 1.04

OVERVIEW

The D8259 is a soft Core of Programmable Interrupt Controller. It is fully compatible with the 82C59A device. The D8259 Core manages up to 8-vectored priority interrupts for processor. Programming it to cascade allows for up to 64 vectored interrupts. More than 64 vectored interrupts can be accomplished by programming to Poll Command Mode.

D8259 can operate in all 82C59A modes, and supports all 82C59A features:

- MCS-80/85 and 8088/8086 processor modes
- Fully nested mode and special fully nested mode
- Special mask mode
- Buffered mode
- Pool command mode
- Cascade mode with master or slave selection
- Automatic end-of-interrupt mode
- Specific and non-specific end-of-interrupt commands
- Automatic and Specific Rotation
- Edge and level triggered interrupt input modes
- Reading of interrupt request register (IIR) and in-service register (ISR) through data bus.

- Writing and reading of interrupt mask register (IMR) through data bus

KEY FEATURES

- 8 vectored priority interrupts
- Up to sixty-four vectored priority interrupts with cascading
- Support for all 82C59A modes features
 - MCS-80/85 and 8088/8086 processor modes
 - Fully nested mode and special fully nested mode
 - Special mask mode
 - Buffered mode
 - Pool command mode
 - Cascade mode with master or slave selection
 - Automatic end-of-interrupt mode
 - Specific and non-specific end-of-interrupt commands
 - Automatic and Specific Rotation
 - Edge and level triggered interrupt input modes
 - Reading of interrupt request register (IIR) and in-service register (ISR) through data bus
- Fully synthesizable, static design with no internal tri-states

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, One Year licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

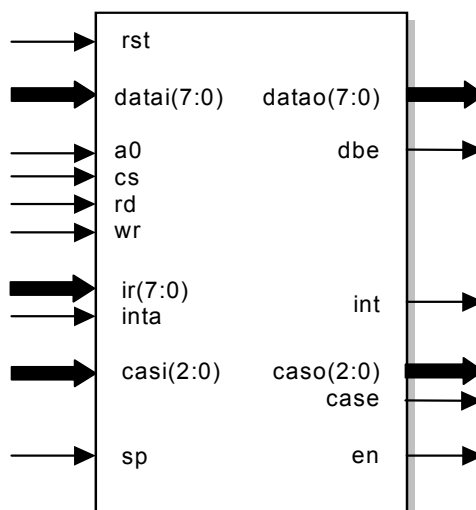
In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except One Year license where time of use is limited to 12 months.

- Single Design license for
 - VHDL, Verilog source code called HDL Source
 - Encrypted, or plain text EDIF called Netlist
- One Year license for
 - Encrypted Netlist only
- Unlimited Designs license for
 - HDL Source

All trademarks mentioned in this document are trademarks of their respective owners.

- Netlist
- Upgrade from
 - HDL Source to Netlist
 - Single Design to Unlimited Designs

SYMBOL



PINS DESCRIPTION

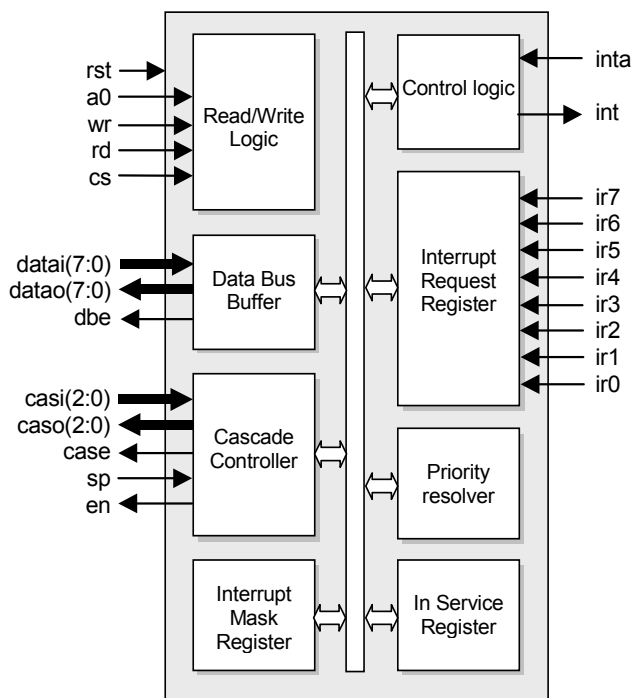
| PIN | TYPE | DESCRIPTION |
|------------|--------|---------------------------|
| rst | input | Power-up reset |
| datai(7:0) | input | Data bus (input) |
| a0 | input | Processor address line |
| cs | input | Chip select |
| rd | input | Read strobe |
| wr | input | Write strobe |
| ir(7:0) | input | Interrupt request lines |
| inta | input | Interrupt acknowledge |
| casi(2:0) | input | Cascade input lines |
| sp | input | Slave program input |
| datao(7:0) | output | Data bus (output) |
| dbe | output | Data bus output enable |
| int | output | Interrupt request output |
| caso(2:0) | output | Cascade output lines |
| case | output | Cascade output enable |
| en | output | Buffer transceiver enable |

<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

BLOCK DIAGRAM

Read Write Logic - The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the D8259. A "low" on the RD input tells the D8259 that the CPU is reading contents of IRR and ISR registers. A "low" on the WR input tells the D8254 that the CPU is writing a Command Words to D8259. Both RD and WR are qualified by CS; RD and WR are ignored unless the D8259 has been selected by holding CS low.

Data Bus Buffer 8-bit buffer is used to interface the D8259 to the system bus.



Cascade Controller - The Cascade Controller stores and compares Identifiers of all 8259 devices in the system. Block manages direction of CAS input/output buses, depending of device status: Master or Slave. When operating as a master the D8259 drives onto the CAS bus address of interrupting 8259 device, then the addressed 8259 slave during the next one or two consecutive INTA pulses send to the Data Bus preprogrammed address of subroutine.

Interrupt Mask Register – IMR register stores the information which interrupt request to be masked.

Control Logic – CL block checks for INTA pulses, which cause the D8259 to release vectoring information onto the Data Bus. Format of drive data depends on mode of operation. CL also manages state of INT output.

Interrupt Request Register – IIR register stores information about states of all IR lines. It saves information about all interrupt requests to be serviced.

Priority Resolver – PR block resolve which interrupt request has the highest priority, and will be served as first.

In Service Register– ISR register stores information about interrupts that are being serviced.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

| Device | Speed grade | Logic Cells | F _{max} |
|-----------|-------------|-------------|------------------|
| CYCLONE | -6 | 394 | 154 MHz |
| CYCLONE 2 | -6 | 387 | 163 MHz |
| STRATIX | -5 | 394 | 164 MHz |
| STRATIX 2 | -3 | 294 | 239 MHz |
| STRATIXGX | -5 | 394 | 166 MHz |
| MERCURY | -5 | 435 | 181 MHz |
| EXCALIBUR | -1 | 407 | 99 MHz |
| APEX II | -7 | 407 | 136 MHz |
| APEX20KC | -7 | 407 | 110 MHz |
| APEX20KE | -1 | 407 | 93 MHz |
| APEX20K | -1V | 407 | 72 MHz |
| ACEX1K | -1 | 413 | 78 MHz |
| FLEX10KE | -1 | 413 | 76 MHz |

Core performance in ALTERA® devices

CONTACTS

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check <http://www.dcd.pl/apartn.php>