UHF Transceiver

PRM 4515U

Technical Manual

Racal-Tacticom Limited

P.O. Box 112, 472 Basingstoke Road, Reading, Berks. RG2 0QF
Tel: Reading (0734) 875181 Telex: 848011

Prepared by Group Technical Handbooks Department, Racal Group Services Limited

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RACAL TACTICOM LIMITED

Amendment to

Technical Manual

for

UHF TRANSCEIVER PRM 4515U Ref TH7158 Issue 1 Dec 86

380 to 400 MHz band

This band has been added to frequency range options available, and is preset by software 29839-979-03 (ML7 on Control Board) which overrides the frequency band selection links LK1, LK2, LK3 and LK4 specified in Table 2 in Chapter 4. This band will be indicated by letter code P (shown after 'PRM4515U' on the nameplate).

An additional feature available on this version is infinite Transmit Timeout option which is selected when pin 13 of IC5 on the Transceiver board is grounded. It overrides setting of LK5 and LK6 (Chapter 4, Table 3). When Pin 13 of IC5 is connected to 5VC on the Transceiver Board, timeout options of 30, 60, 90 and 120 secs as mentioned in the manual are selected as specified.

The helical antenna required for this band is 29280-052-10.

FL3 and FL4 helical filters are: 27241-009-00
RX VCO (4b) Module is : 49301-200-14
TX VCO (4c) Module is : 49301-198-14

The manual should be amended as follows:

Tech Spec 1

Frequency range to read:
380 to 400 MHz or 403 to 471 MHz in specified 20 MHz band, 4 MHz resolution.

Page 1-1

Paragraph 1 line 3 to read:
.... clear data communication over 380 MHz to 400 MHz band or a (predefined) 20 MHz segment 403 MHz to 471 MHz (UHF) band.

Page 2-2

Paragraph 6 line 1 to read:
The operating frequency range is either 380 to 400 MHz or a 20 MHz band in the range 403 to 471 MHz, in 4 MHz steps ....

Page 3-6

Paragraph 19 (10) to read:
Antenna, 29280-050-10 or 29280-051-10 or 29280 052-10.

Page 3-7

Paragraph 21 last line add:
P - 380

Page 4-13

TABLE 1 Signal column add bracket for first five inputs (P1-P5) and the following:
Applicable to 403 to 471 MHz only

Page 4-14

TABLE 2 Note now to read:
Notes 1. Other link combinations are not used by PRM4515U.
2. For 380 to 400 MHz, microcomputer software overrides above links.

TABLE 3 add Note:
For 380 to 400 MHz microcomputer software overrides above links and sets timeout to infinity if P5 is held low. If P5 is held high then above timeout options apply.

Page 5-27

Test No 20.1 add
P : 380 MHz
line under table to read:
In 4 MHz steps from 403(A) to 451(N).

Page 9-10

Add line to table:
380-400 P 27241-009-00 49301-200-14 49301-198-14

Page 9-16

ML7 to read:
ML7 Programmed Microprocessor 403-471 MHz 29839-990-60
380-400 MHz 29839-979-03

BERYLLIUM OXIDE - SAFETY PRECAUTIONS

INTRODUCTION

Observe the following safety precautions when handling components that contain beryllium oxide. Most RF transistors contain this material although the beryllium oxide is not visible externally.

PRACTICAL PRECAUTIONS

Beryllium oxide is dangerous in dust form when it can be inhaled or enter a cut or irritation area. Take reasonable care not to generate dust by abrasion of the material.

Power Transistors

There is normally no hazard with power transistors as the beryllium oxide is encapsulated within the devices. They are safe to handle for replacement purposes, but when removing defective items, ensure that they do not become physically damaged:

(a) Do not carry them loosely in a pocket, bag or container with other components where they may rub together or break and disintegrate into dust;

(b) Do not heat them excessively (normal soldering is safe);

(c) Do not break them open for inspection or in any way abrade them with tools.

DISPOSAL

Do not dispose of defective and broken components in containers used for general refuse. Individually wrap them, clearly identified as "DEFECTIVE BERYLLIUM COMPONENTS" and return them to the Equipment Manufacturer for subsequent disposal.

Individually wrap broken components and identify them as "BROKEN BERYLLIUM COMPONENTS". Do not send them through the post; return them by hand.

MEDICAL PRECAUTIONS

If beryllium is believed to be on or to have entered the skin through cuts or abrasions, thoroughly wash the area and treat it with normal first aid methods, followed by medical inspection.

Suspected inhalation requires treatment, as soon as possible, by a doctor (preferably at a hospital).

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CMOS HANDLING PRECAUTIONS

The input impedance of a CMOS device is of the order of 10^{14} ohms. The breakdown voltage of the oxide within the device is about 100 volts. As static voltages of up to 4kV can be generated by silk, nylon or plastic clothing or containers, it is essential that precautions are taken to prevent high voltages occurring at the leads of CMOS devices, as follows:

(1) Earth the tips of soldering irons to the earth plane of the board being soldered.

(2) Do not store the devices in plastic bags or containers (unless the plastic has been specially treated with anti-static chemicals).

(3) Do not wear nylon or plastic gloves, or rubber-soled shoes.

(4) Short as many leads as possible, with the fingers, during handling.

(5) Do not remove the input connection with the device connected to the supply rail.

Note that VMOS FETs are particularly sensitive to static.

SOLVENTS

Do not allow solvents used for cleaning purposes (e.g. after a pcb repair) to come into contact with the plastic switches.

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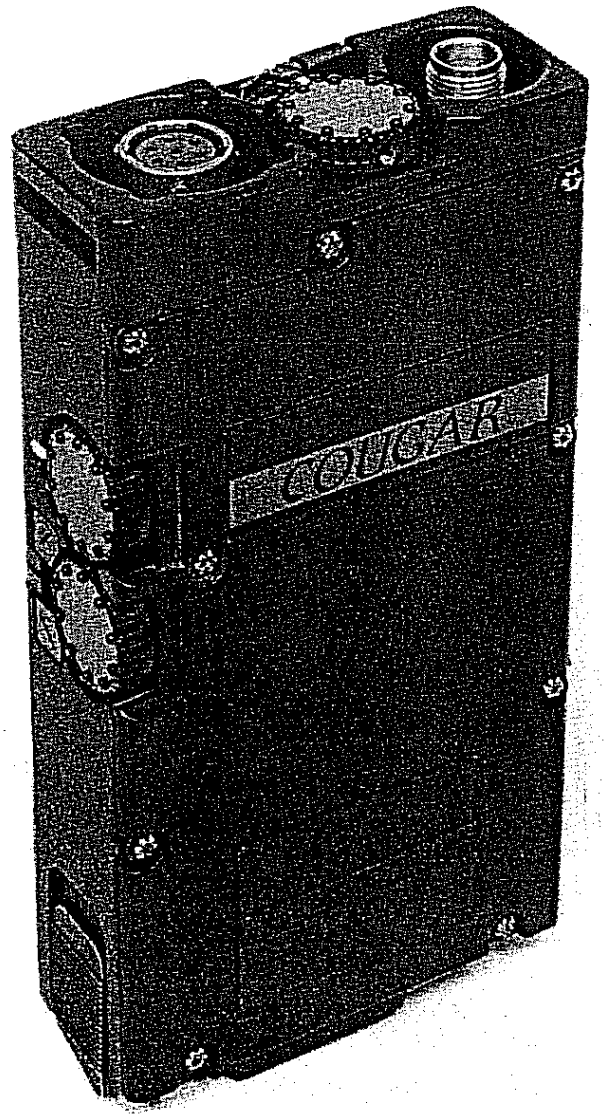

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PRM 4515U UHF Transceiver

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PRM4515U UHF TRANSCEIVER

CONTENTS

TECHNICAL SPECIFICATION

CHAPTER 1 GENERAL DESCRIPTION

CHAPTER 2 OPERATING INSTRUCTIONS

CHAPTER 3 OVERALL DESCRIPTION AND PERFORMANCE CHECK

CHAPTER 4 TRANSCEIVER BOARD

CHAPTER 5 CONTROL BOARD

CHAPTER 6 CRYPTO BOARD

CHAPTER 7 INTERCONNECTIONS, SWITCH AND DECOUPLING BOARDS

CHAPTER 8 DISMANTLING, FAULT LOCATION AND ALIGNMENT

CHAPTER 9 COMPONENTS LIST

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TECHNICAL SPECIFICATION

GENERAL

Frequency Range	403 to 471 MHz. Specified 20 MHz band, 4 MHz resolution.
Channels	10 programmable (1 or 2 frequency simplex).
Channel Spacing	25 kHz.
Frequency Steps	12.5 kHz.
Frequency Stability	Better than ±5 ppm over the specified temperature and supply range (figure does not include aging, which is 2 ppm per annum maximum).
Operating modes	F3E (narrowband FM) simplex or two frequency simplex. F1E 16k bit/sec data.
Performance	Generally complies with requirements of MPT 1301.
Supply	10V dc nominal.
Encryption	Internal 16k bit/sec speech security system.
RF Connector	50 ohm TNC socket.

TRANSMITTER

Power (into 50 ohms)	2W +2 -1 dB (>9.6V supply).
Harmonics	Below -70 dB relative to carrier.
Peak Deviation	±5 kHz maximum.
Squelch Tone	150 ±2 Hz in clear mode.
AF Response: Narrowband (Voice) Wideband (Data)	400 Hz to 2.7 kHz within 6 dB. 30 Hz to 10 kHz within 6 dB.

Spurious Emissions	Below -70 dB relative to carrier.
Adjacent Channel Power:	
Clear Mode	Below -55 dB relative to carrier.
Secure Mode	Below -45 dB relative to carrier.

RECEIVER

Maximum Usable Sensitivity:	
Narrowband	Application of 0.35 µV pd maximum at the receiver input at the nominal frequency of the receiver, with ±3 kHz deviation at 1 kHz produces an audio output with SINAD of 12 dB.
Clear, External Wideband Data	Less than 10% synchronous bit error rate at 0.35 µV pd.
Maximum AF Output Power	10 mW into 300 ohms, 400 mW into 8 ohms.
AF Response: Narrowband	400 Hz to 2.7 kHz within nominally 6 dB.
Wideband	30 Hz to 8 kHz within nominally 6 dB.
Image Rejection	Better than 65 dB.
IF Rejection	Better than 70 dB.
Spurious Response Rejection (External)	Better than 70 dB.
Spurious Emission in Receive Mode	Does not exceed 20 nW.
Squelch: Clear Mode	150 Hz tone.
Secure Mode	16k bit/sec.
Adjacent Channel Selectivity	Better than 60 dB.
Volume Control	6 stepped volumes.
Intermodulation Response Rejection	Better than 60 dB.
Blocking Level	Better than -23 dBm.

POWER REQUIREMENTS

Current Consumption:

Transmit	600 mA typical.
Receive	55 mA typical.
Standby	50 mA typical.

DIMENSIONS

Height	150 mm. 213 mm with MA4516A battery.
Width	75 mm.
Depth	30 mm.
Weight	450 g (approximately). 800 g with MA4516A battery.

ENVIRONMENT

Temperature: Full specification	$-20^{o}C$ to $+55^{o}C$.
Storage	$-40^{o}C$ to $+85^{o}C$.
Immersion/Humidity	Case sealed. To Mil 810C Section 512.1 Proc I.

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CHAPTER 1

GENERAL DESCRIPTION

CONTENTS

	Page
INTRODUCTION	1-1
OPERATION	1-1
Transmit	1-1
Receive	1-2
Whisper	1-2
Squelch-Open (Noise-On)	1-2
Wideband Data	1-3
Fixed Level Audio	1-3
Wrong Switch Setting	1-3
Channel Frequencies	1-3
Cipher Codes	1-3
Power Saving	1-3
CONSTRUCTION	1-4
INTERFACE CONNECTIONS	1-4
ANCILLARIES	1-5

TABLES

Table No.		
1	Functions of Connections to AUDIO Socket	1-4

ILLUSTRATIONS

Fig. No.	
1.1	Audio Connector Details
1.2	PRM4515U : Construction (1)
1.3	PRM4515U : Construction (2)
1.4	PRM4515U with Battery and (typical) Handset plus Antenna

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1 The PRM4515U UHF Transceiver is a hand-held FM radio transmitter/receiver, with optional built-in voice encryption. It allows secure speech, clear speech and clear data communication over a (predefined) 20 MHz segment of the 403 MHz to 471 MHz (UHF) band. The unit operates on ten channels and the transmit and receive frequencies for each channel are set individually, so single or two-frequency simplex operation is available on each channel. Frequencies and cipher codes are entered from an external programmer or fill gun device. The PRM4515U can interface with UHF Amplifier TA4523U, which increases its range, and Extended Control Unit MA4730, which allows remote control, and forms the basis of a static/mobile/transportable area coverage communications system.

OPERATION

2 To operate, the PRM4515U has an antenna connected to the RF connector, and a loudspeaker/microphone or handset/headset with PTT/Pressel facility connected to the audio socket. The connections can be made directly, or indirectly via associated equipment. Power is provided by a clip-on battery (MA4516A or MA4516B) or from an external source via associated equipment. The selected frequency of a receiving unit must be the same as the selected frequency of a sending unit, and, for secure communication, the receiver and transmitter must use the same cipher code. Full details of controls, indicators and operating instructions are given in Chapter 2.

Transmit

3 To transmit a message, the operator switches the OFF/Volume switch to any position except OFF, sets the Channel switch to the required channel number, and the Mode switch to either CLR (for clear operation), A (for secure operation using one of the stored cipher codes) or B (for secure operation using the other stored cipher code). The operator then activates PTT/Pressel and starts to send the message. If secure transmission is selected, the crypto encrypts the message, producing a 16k bit/sec data stream containing sync codes which allow the receiving unit to synchronise its timing

and decoding circuits. If clear transmission is selected, the message bypasses the crypto circuit; the unit adds a 150 Hz squelch tone to indicate the presence of a valid message and sends a slow-pip warning back to the operator to indicate that the transmission is not secure.

4 A processor automatically sets the frequency synthesiser to produce the transmit frequency stored against the selected channel number, and the clear or encrypted audio signal modulates this frequency. The power amplifier boosts the FM signal to drive the antenna. While the unit is transmitting, the Transmit indicator is illuminated. When PTT is activated it starts a preset timer which limits transmission time; five seconds before the end of the allowed time, the unit sends rapid pips to the operator, then, at time-out, terminates the transmission and sends the operator a two-tone warning. To continue to transmit, the operator must activate PTT/Pressel again.

Receive

5 The unit can receive a message at any time, provided it is switched-on and is not transmitting. The synthesiser produces the local oscillator frequency which is mixed with the incoming signal to produce a modulated signal at 21.4 MHz. This is the first intermediate frequency, at which the signal is amplified. A second mixer produces a modulated signal at the second IF frequency, 455 kHz, and, from this, the FM detector extracts the audio signal. The unit then detects either the 16k bit/sec pattern and sync code of a secure signal, which it decrypts, or the 150 Hz squelch tone of a clear message, which bypasses the decryption circuits. The OFF/Volume control adjusts the level of the audio signal and the audio power amp boosts the audio output. The processor adds a slow-pip warning to a received clear signal.

Whisper

6 If the operator has selected whisper mode (either of the first two OFF/Volume switch positions after it has been turned clockwise from the OFF position), the unit increases the microphone sensitivity to allow normal transmit operation with a whispered input to the microphone, and provides a very low level audio output when a received signal arrives.

Squelch-Open (Noise-On)

7 The operator can select squelch-open (either of the last two OFF/Volume switch positions, marked ● and ✱), which allows the operator to hear anything that is on the selected channel (e.g. clear signals that do not have the 150 Hz squelch tone).

Wideband Data

8 When data equipment is connected to the audio socket and the WIB signal to the Transceiver is activated, incoming data on the Mic line bypasses the audio processing and encryption circuits of the transmitting unit. Likewise, in a receiving unit externally-programmed for wideband, the data bypasses the decryption and audio circuits.

Fixed Level Audio

9 A fixed high-level audio output can be externally-programmed. When the FLA input signal is active, a receiving unit produces an audio output at a fixed level (suitable for volume control by external equipment).

Wrong Switch Setting

10 If the unit receives a clear signal when it is set for secure operation, it automatically switches to clear mode and outputs the received signal with slow-pip warning tones. If it receives a secure signal while set for clear operation (and has a crypto fitted), it outputs 'white noise' (still-encrypted message); the operator can then select the appropriate secure mode to decrypt the remaining message.

Channel Frequencies

11 Twenty frequencies, ten for transmit, ten for receive, are entered by an external device (via the line normally used for PTT), and the frequency information is stored against channel numbers. For each transmit operation the processor loads the synthesiser with the selected transmit frequency information, and, after the end of the transmission, reloads the corresponding receive frequency information in case a reply is received.

Cipher Codes

12 Two cipher codes, A and B, are entered by an external device (via the line normally used for PTT) and the codes are stored in the crypto module. The receiving unit can decrypt a secure message only if it uses the same code that was used by the transmitting unit. Code storage requires power, but a built-in facility allows the codes to be stored (for at least fifteen minutes) while the battery is changed.

Power Saving

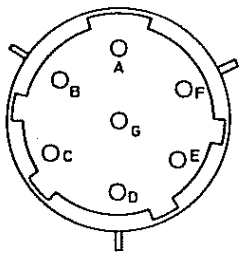
13 The microprocessor controls the distribution of power in the unit. It switches-on only the parts of the circuits that are required for a particular selected mode of operation and thus prolongs battery life. When the unit is switched-on but not actually transmitting or receiving a message, it monitors battery power, and produces an audible warning (noise bursts) for the operator when power is low.

CONSTRUCTION

14 The unit is constructed on a cast aluminium chassis, as shown in Figs. 1.2 and 1.3. The RF and audio sockets, OFF/Volume, Channel and Mode controls fit directly onto the chassis. The Control Board is secured to the centre of the chassis, with the Crypto Board and Transceiver Board plugged-in alongside. Three small printed circuit boards plug into the backs of the three switches and one connects to the audio socket. The small boards have flexible-strip connections to the Control Board. Two removable covers, secured by captive screws, seal the unit. A pressure test hole, normally blocked by a sealing screw, allows the unit sealing to be checked. Signals to/from the antenna go via the coaxial RF socket, all other signals, audio, control, frequency data and cipher codes, go via the seven-way audio socket. The battery input contact is at the other end of the unit.

INTERFACE CONNECTIONS

15 The RF connector is a 50 ohm RF socket type TNC. The signals that use the seven-way audio connector are detailed in Table 1.



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62GB-10F-10-07 SN.

Fig 1.1 Audio Connector Details

TABLE 1

Functions of Connections to Audio Socket

Pin	Signal	Function
A	Mic	(1) Microphone input. Normal voice 1 mV rms, Whisper 0.25 mV rms.
		(2) Wideband Data input. 1.3V peak-to-peak.
		(3) Fixed Level Audio program input. 1 mA selects FLA.
B	Mic Return	(1) Microphone return, ac-coupled to 0 V.
		(2) Wideband program input. 1 mA selects wideband mode.

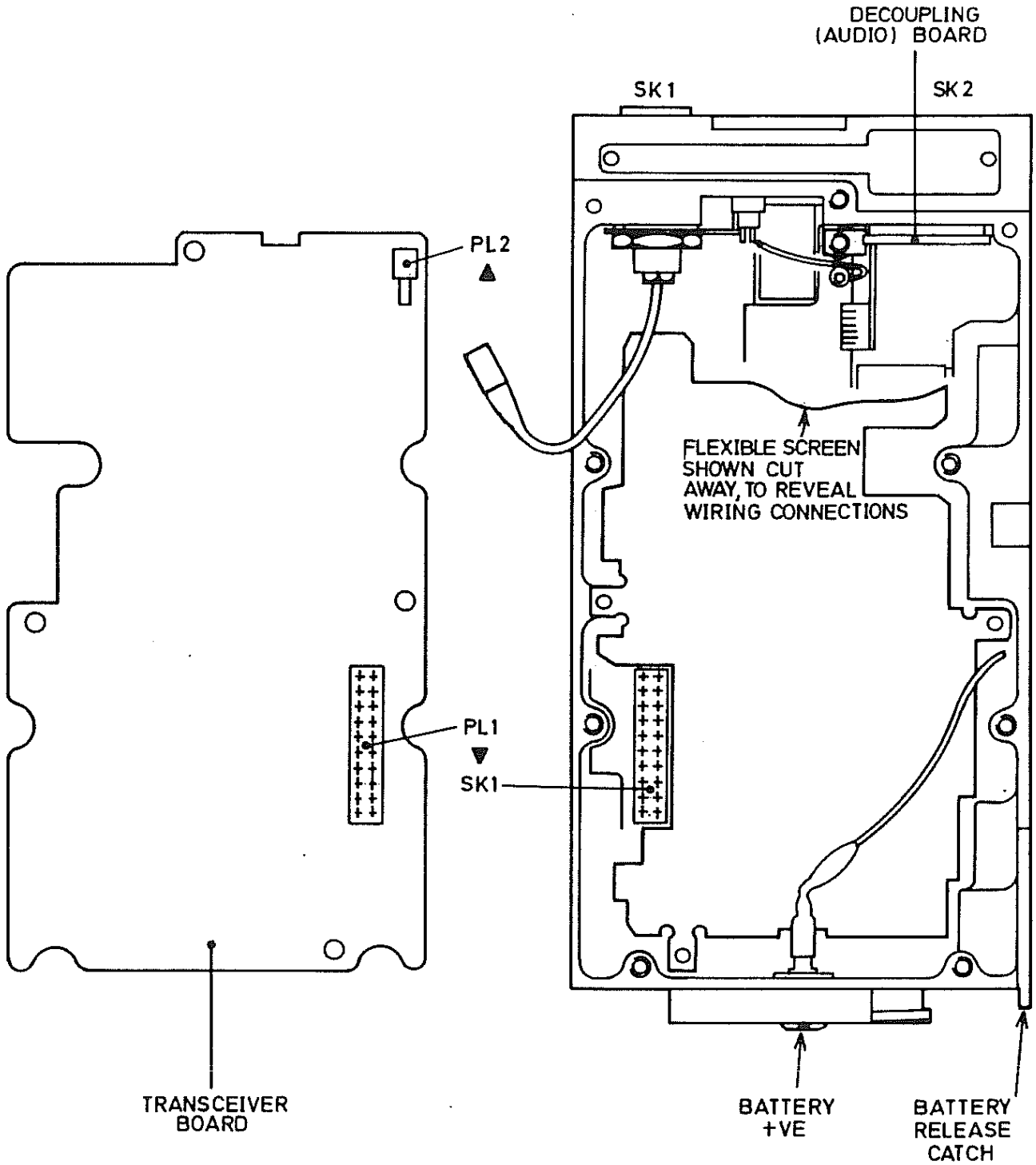
TABLE 1 (Continued)

Pin	Signal	Function
C	10V	Supply in or out. Input overvoltage protected. Output current-limited to 100 mA (nominal).
D	Audio/Data	(1) Audio output, variable to 5V peak-to-peak. (2) Wideband data output. 5V peak-to-peak. (3) Audio output, 5V peak-to-peak (FLA).
E	Earth	Connected to chassis and OV.
F	PTT/Serial Data	(1) Press to Talk input. Less than 3.5V for longer than 1 ms selects transmit mode. (2) Serial Data input and output. 4k bit/sec serial data, logic high 5.5V, logic low 3.5V.
G	Squelch/CTS	(1) Squelch output. 1 mA when a valid squelch (150 Hz tone or 16k bit/sec data) is received, or the unit is set for squelch-open. (2) Clear To Send output. 1 mA when the unit is clear to send in transmit mode.

ANCILLARIES

16 The following equipment is available for use with the PRM4515U:

UHF Amplifier	400-440 MHz:	TA4523UA
	420-471 MHz:	TA4523UB
Rechargeable Battery		MA4516A
Battery (Primary)		MA4516B
Loudspeaker/Microphone with Antenna Socket		712432
Loudspeaker/Microphone		791745
Headset (Boom mic)		712372
Handset		712433
UHF Helical Whip Antenna	400-440 MHz:	29280-051-10
	420-471 MHz:	29280-050-10
Cable, RF: PRM4515U to TA4523U		791702
Cable, Audio/DC: PRM4515U to TA4523U		791715
Battery Charger, Single-Way		MA4517A
Battery Charger, Six-Way		MA4518A
Programmer		MA4073B
Frequency Fill Gun		MA4083B
Cable, Control: Programmer/Fill Gun to PRM4515U		791641



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PRM 4515U: Construction (1)
(side covers removed)

Fig.1.2

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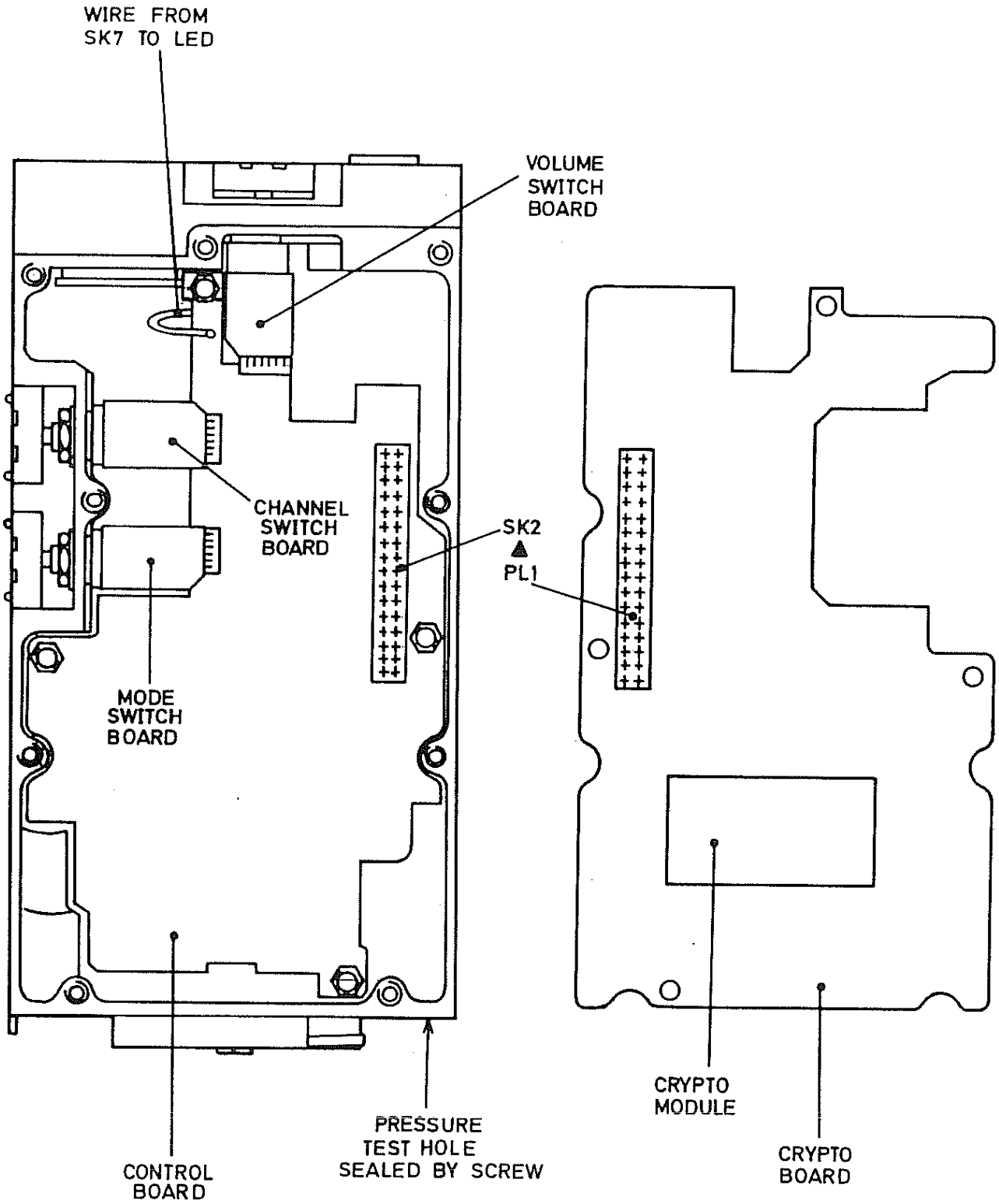

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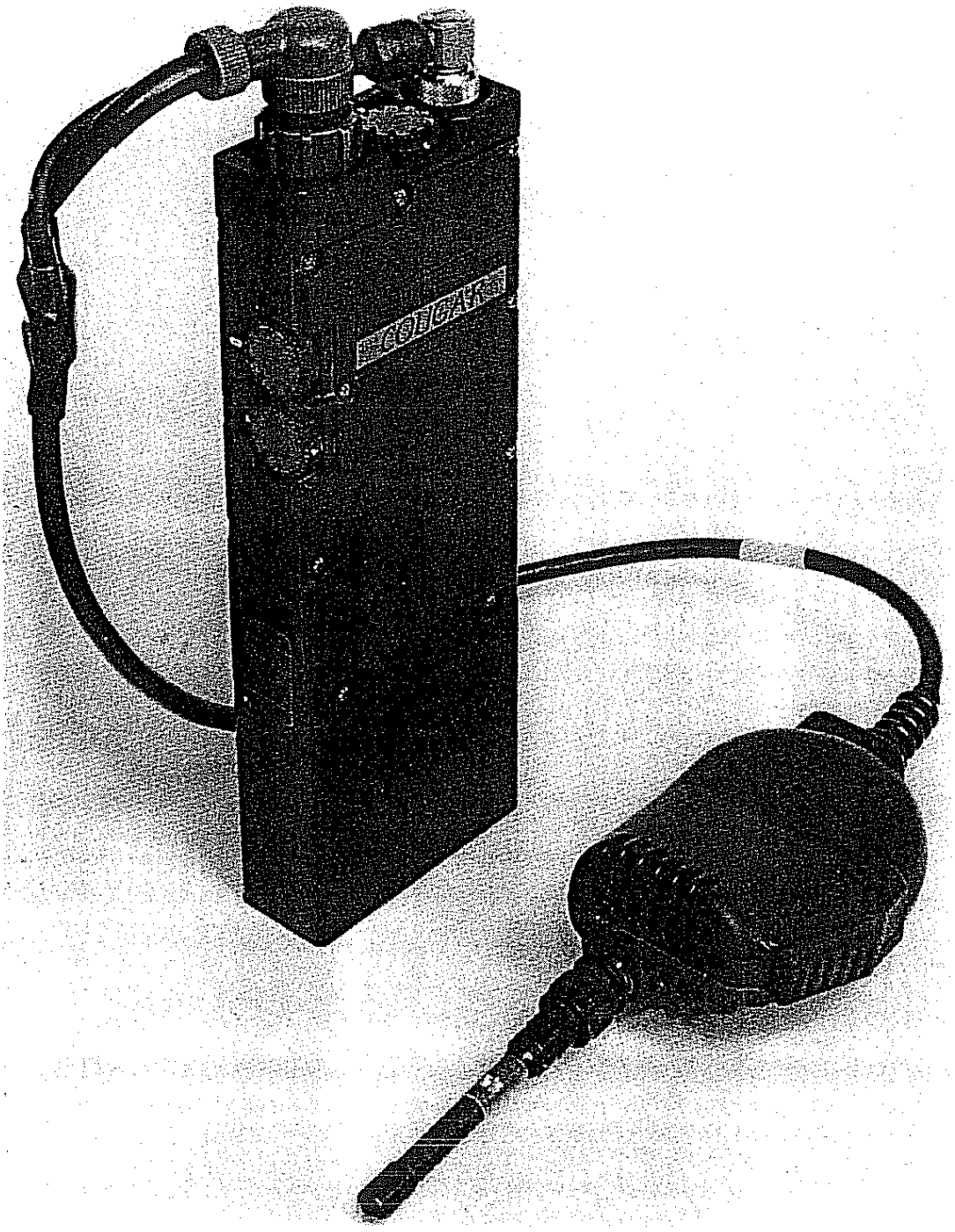
PRM 4515U: Construction (2)
(side covers removed)

Fig.1.3



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PRM 4515U with Battery and (Typical) Handset Plus Antenna

Fig.1.4

CHAPTER 2

OPERATING INSTRUCTIONS

CONTENTS

	Page
CONTROLS AND INDICATORS	2-1
OFF/Volume Switch	2-1
Channel Switch	2-2
Mode Switch	2-2
Transmit Indicator	2-2
OPERATING FREQUENCY RANGE	2-2
PRESET OPTIONS	2-2
OPERATING INSTRUCTIONS	2-4
Loading Frequencies	2-4
Loading Cipher Codes	2-4
Cipher Code Erasure	2-4
Switch-on/Standby	2-4
Transmit	2-5
Receive	2-5
Alarm and Warning Signals	2-5
Battery Fitting/Removing	2-6
Use with Associated Equipment	2-6
OPERATOR'S ROUTINE MAINTENANCE	2-6
Functional Check	2-6
Battery Check	2-8

TABLES

Table No.

1	OFF/Volume Switch Functions
2	Mode Switch Functions

ILLUSTRATIONS

Fig. No.

2.1	PRM4515U : Controls and Indicators

CHAPTER 2

OPERATING INSTRUCTIONS

CONTROLS AND INDICATORS

1 There are three switches, one mechanical interlock and one indicator on the PRM4515U, shown in Fig. 2.1.

OFF/Volume Switch

2 The OFF/Volume switch is a nine-position rotary switch. The most counter-clockwise position is OFF.

TABLE 1

OFF/Volume Switch Functions

Position	Symbol	Function
0	OFF	Off.
1		Low level audio output, and the unit amplifies whisper-level microphone inputs to normal transmit output levels.
2		As position 1, but with a higher audio output.
3		Increasing audio output levels as switch turns clockwise. (Standard amplification of microphone input.)
4		
5		
6		
7		Squelch open (noise-on). Unit does not require the detection of a 150 Hz squelch tone or 16k bit/sec data in the incoming signal: it continuously outputs the received signal, at a volume equivalent to switch position 3.
8		As position 7, but at maximum volume.

Channel Switch

3 The Channel switch is a ten-position rotary switch. Each of the positions, 0 to 9, selects a stored transmit frequency and a stored receive frequency. The most counter-clockwise position is 0.

Mode Switch

4 The Mode switch is a four-position rotary switch. The most counter-clockwise position is normally CLR, but when the mechanical interlock is operated, the switch can be turned further to the Z position.

TABLE 2

Mode Switch Functions

Symbol	Function
CLR	Clear mode operation.
A	Secure mode operation, using stored cipher code A.
B	Secure mode operation, using stored cipher code B.
Z	Erase (zeroise) stored cipher codes A and B. Protected by a mechanical interlock.

Transmit Indicator

5 The Transmit indicator is illuminated when the unit is transmitting. It flashes when transmit power is low. A sliding cover is fitted over the indicator.

OPERATING FREQUENCY RANGE

6 The operating frequency range is a 20 MHz band in the range 403 to 471 MHz, in 4 MHz steps (selected by links on the Transceiver Board: for details see Chapter 4, Para. 32). The unit accepts and stores only frequencies that are within its selected operating range: when an attempt is made to load out-of-range frequencies it ignores them (and this causes the loading device to indicate a load failure).

PRESET OPTIONS AND ADJUSTMENTS

7 Link options and adjustable components inside the unit are preset during manufacture to suit the particular system: no further action is required before use.

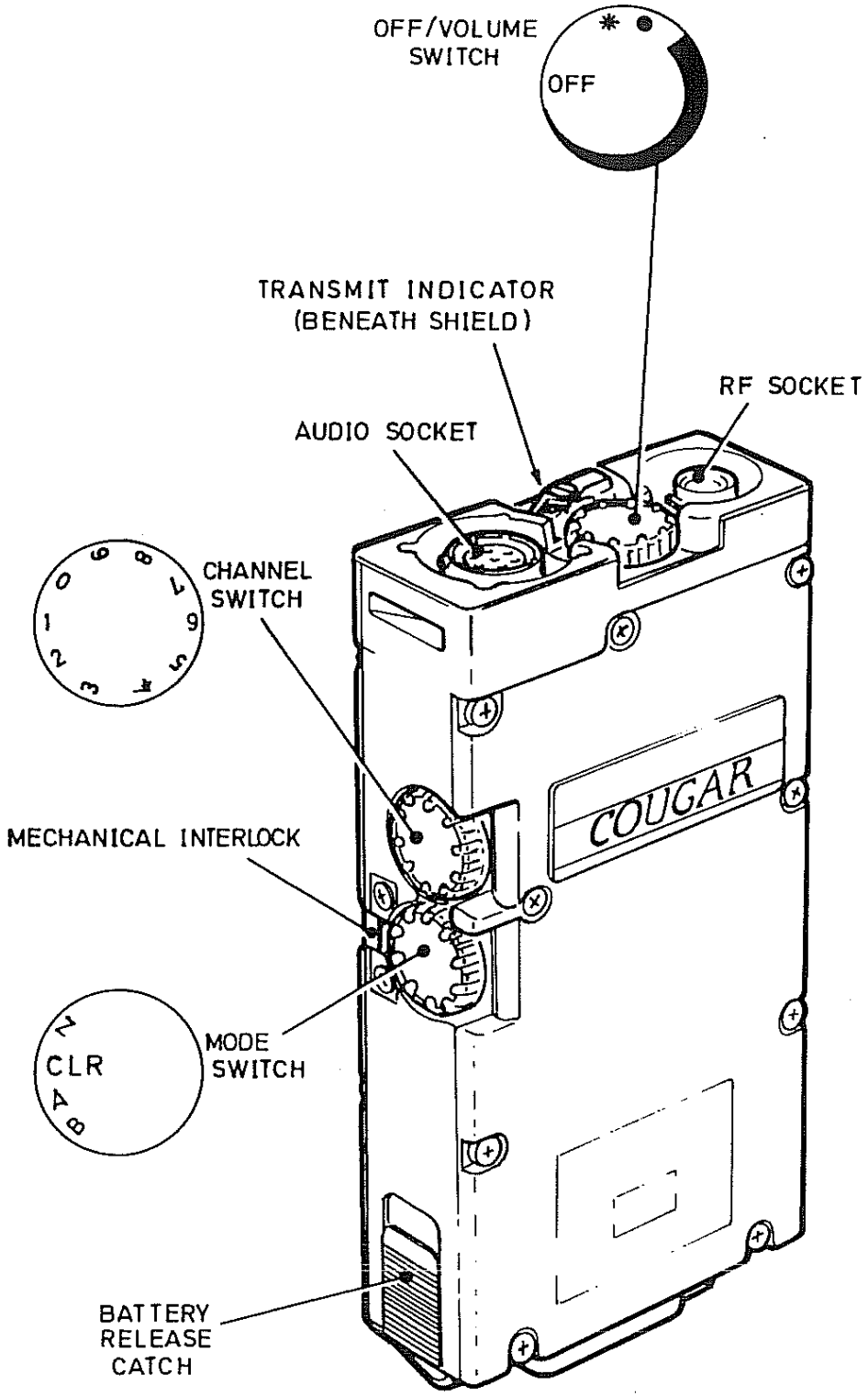


Fig 2.1 PRM4515U: Controls and Indicators

OPERATING INSTRUCTIONS

8 The basic operating instructions, Paras. 8 to 25, apply to a PRM4515U powered by a clip-on battery, and with an antenna and loudspeaker/microphone or handset/headset with PTT facility connected.

Loading Frequencies

9 Frequencies are loaded with the fill device connected to the unit's audio socket (in place of the handset/phones etc) and the unit switched-on (OFF/Volume switch at an on-position). Follow the load procedure given in the user handbook or the technical manual for the fill device.

Loading Cipher Codes

10 Cipher codes are loaded with the fill device connected to the unit's audio socket (in place of the handset/phones etc), the antenna disconnected, and the unit switched-on but not with squelch-open (ie. the OFF/Volume switch should be at position 1 to 6).

(1) Set the Mode switch (on the Transceiver) to Z to erase the stored codes, then return it to A.

(2) Follow the load procedure given in the user book or the technical handbook for the fill device.

11 The codes are retained while a charged battery is fitted, regardless of whether the unit is switched on or off. Also, the codes are retained for at least fifteen minutes after the battery has been removed (but typically for several hours). However, if the battery is completely discharged or removed, unless a serviceable battery is fitted in time, the codes are lost.

Cipher Code Erasure

12 To erase the cipher codes stored in the unit, press and hold-in the mechanical interlock and briefly set the Mode switch to Z (zeroise). The unit does not need to be switched-on nor to have power supplied for this operation.

Switch-on/Standby

13 Select the required channel number (0 to 9). Set the Mode switch to CLR (clear) or A or B (secure) as required. Set the OFF/Volume switch to the required volume (or whisper or squelch-open) position. The unit is now in standby mode: it automatically receives at any time (unless transmitting) and transmits on receipt of PTT. If it produces a chuff-chuff noise (bursts of receiver noise) at the audio output, the battery is low. Change the battery (Para. 24).

Transmit

14 To transmit, activate PTT/Pressel. While PTT is activated, the unit transmits and the Transmit indicator is illuminated. If the transmission is in clear mode the unit produces slow pips at the audio output. For the last 5 seconds before the transmit timer times-out and terminates the transmission, the unit produces rapid pips at the audio output. After time-out, the unit outputs a continuous two-tone (alternating) signal until PTT is deactivated. To continue transmitting, reactivate PTT. Transmit time is preset to 30, 60, 90 or 120 seconds (Chapter 4, Para. 31). If the Transmit indicator flashes while the unit is transmitting, the battery is low. Change the battery.

Receive

15 When receiving a clear signal the unit adds slow pips to the signal it outputs to the loudspeaker. This applies whether the unit is set for clear or secure operation.

16 When receiving a secure signal, if set for the correct secure mode (A or B), the unit outputs the decrypted signal. If the unit is set for clear operation, it outputs a received secure signal as 'white noise' (i.e. still encrypted). Set the Mode switch to A or B as applicable to decrypt the message.

Alarm and Warning Signals

17 The following paragraphs (18 to 23) summarise the alarm and warning signals generated by the unit.

18 Continuous tone (secure modes (A and B) only). Failure in cipher circuits prevents the unit from transmitting. The fault may clear if PTT is reactivated or if the secure mode is switched from A to B (or vice versa) and back again. If the tone continues, use the unit only in clear mode.

19 Continuous two-tone.

(1) Transmit time limit has been exceeded: deactivate PTT.

(2) No crypto module fitted in unit: use clear mode only.

(3) The selected frequency is not working: switch off then on again and re-try the channel. Other channels may be useable.

20 Transmit indicator flashing in transmit mode or short pulses of noise output in standby mode. The battery is low. The unit transmits with reduced power but receives normally. Change the battery.

21 White noise output in clear mode. The unit is receiving a secure signal. Switch to secure mode A or B, as applicable, to decrypt the message (provided the unit has the required cipher code).

22 Short pips at two-second intervals. The unit is transmitting or receiving a clear signal.

23 Rapid pips. Last five seconds of transmit time.

Battery Fitting/Removing

24 (1) Set the OFF/Volume switch to OFF.

(2) Locate the battery in position on the bottom of the unit, and twist it clockwise to lock it to the unit.

(3) To remove the battery, slide back and hold the battery release catch on the unit, then twist the battery anti-clockwise.

Use with Associated Equipment

25 When the PRM4515U is used with associated equipment connected to its audio socket, power, channel numbers and cipher codes, and in some cases frequencies and all control signals, are supplied by or via the associated equipment. Details of operation are given in the applicable user manual.

OPERATOR'S ROUTINE MAINTENANCE

26 The PRM4515U requires very little routine maintenance. At intervals, carry out the following checks:

(1) The unit is complete.

(2) Surfaces are clean and undamaged.

(3) The switches have smooth positive action.

(4) Fittings (sockets, switch knobs, etc.) are secure and undamaged.

Functional Check

27 Carry-out the functional check daily when the unit is in use, and weekly when in store, or when a fault is suspected in the PRM4515U. Operate the unit with known serviceable associated equipment (antenna, ECU, handset, etc.), and exchange messages with another known serviceable system. In the following procedure, the unit under test (UUT) and its associated equipment is the 'local' system, the other system is 'remote'. For the functional check, the local and remote Transceivers must be loaded with the same frequencies and cipher codes.

28 Set the local and remote Transceivers for clear operation (Mode switches set to CLR), on channel 0, with a normal volume setting (OFF/Volume switches not set to Whisper or Squelch-Open positions).

29 Transmit from the remote unit. At the local unit:

(1) Confirm undistorted audio output at the loudspeaker with slow pips.

(2) Confirm correct audio output levels over the range of OFF/Volume switch settings.

(3) Set the Mode switch to A and confirm undistorted audio output with slow pips.

(4) Set the Mode switch to B and confirm undistorted audio output with slow pips.

30 At the local unit, set the OFF/Volume switch to a central position, the Mode switch to CLR, and activate and hold PTT/pressel.

(1) Confirm that the Transmit indicator illuminates.

(2) Confirm that warning pips are heard during the last five seconds before the transmit period times-out.

(3) Confirm that the Transmit indicator is extinguished and a two-tone warning is heard after time-out.

(4) Release PTT/pressel and confirm that the warning signal is removed.

31 Transmit from the local unit and confirm satisfactory signal reception at the remote unit.

32 Transmit from the local unit using whisper mode: set the OFF/Volume switch to position 1 and use a low audible input to the microphone. Confirm satisfactory reception at the remote unit.

33 Repeat the whisper transmission with the OFF/Volume switch set to position 2.

34 Repeat the clear receive and transmit tests (Paras. 29 to 33) using the other channels, 1 to 9.

35 At the remote unit, set the Mode switch to B, and transmit. At the local unit:

(1) Confirm that 'white' noise is heard.

(2) Set the Mode switch to A and confirm that nothing is heard.

(3) Set the Mode switch to B and confirm that undistorted (decrypted) audio is heard.

36 At the remote unit, set the Mode switch to A and transmit. At the local unit confirm that nothing is heard, then set the Mode switch to A and confirm that undistorted (decrypted) audio is heard.

37 Transmit from the local unit and confirm satisfactory (decrypted) signal reception at the remote unit.

38 Set both Mode switches to B, transmit from the local unit and confirm satisfactory reception at the remote unit.

39 At the local unit, set the OFF/Volume switch to OFF and remove the battery. After 15 minutes, refit the battery, switch the unit on and confirm satisfactory secure communication with the remote unit (i.e. confirm that the stored cipher codes have been retained).

40 At the local unit, release the mechanical interlock and set the Mode switch to Z then to A. Activate PTT/pressel and confirm:

(1) A continuous warning tone is heard.

(2) The unit does not transmit a modulated signal (i.e. no message or white noise heard at remote unit).

41 At the local unit, set the Mode switch to B and confirm Paras. 40 (1) and (2).

Battery Check

42 For the battery check the PRM4515U is operated with a PTT/pressel facility connected.

43 Set the OFF/Volume switch to position 6 (maximum volume but not squelch-open). In the standby mode (not transmitting or receiving), confirm that short pulses of noise are not heard.

44 Set the OFF/Volume switch to position 7 (squelch-open) and confirm that noise is heard.

45 Activate PTT/pressel and confirm that the Transmit indicator illuminates continuously (i.e. it does not flash during transmission).

46 If a test fails, change the battery and repeat the tests.

CHAPTER 3

OVERALL DESCRIPTION AND PERFORMANCE CHECK

CONTENTS

	Page
GENERAL	3-1
PRINCIPLES OF OPERATION	3-1
Switch-on	3-1
Standby Mode	3-1
Transmit Secure	3-2
Transmit Clear	3-2
Transmit Wideband (Clear Data)	3-4
Receive Secure	3-4
Receive Clear	3-4
Receive Wideband (Clear Data)	3-5
Receive Squelch-Open (Noise-On)	3-5
Warning Tones	3-5
Frequency, Cipher Codes and Control Data	3-5
OVERALL PERFORMANCE CHECKS	
List of Test Equipment	
Setting-Up	
Programming	
Transmitter Tests	
Receiver Tests	
APPENDIX 1: PERFORMANCE CHECK LIST	

ILLUSTRATIONS

Fig. No.	
3.1	PRM4515U: Block Diagram
3.2	Tx and Rx Signal Routeing
3.3	Test Equipment Configuration for Tx Tests
3.4	Test Equipment Configuration for Rx Tests

CHAPTER 3

OVERALL DESCRIPTION AND PERFORMANCE CHECK

GENERAL

1 The PRM4515U has most of its electronic components on three main printed circuit boards. These boards are described in separate chapters, with detailed principles of operation, technical description, circuit and layout diagram for each board.

2 This chapter describes the overall principles of operation, with an interconnection diagram that shows how the various parts of the unit are electrically connected.

PRINCIPLES OF OPERATION (Fig. 3.1)

Switch-On

3 When the unit is switched-on, the regulators on the Control Board power the 8V and 5V supply rails from the battery supply, and the microprocessor on the Control Board is reset to the start of its program. The processor reads initialise information from latches on the Transceiver Board. This information defines the frequency range in which the Transceiver Board can operate, and the time allowed for each transmission (selected by preset inputs to the latches). It also shows whether or not a crypto module is fitted (defined by a signal from the Crypto Board via the latches). The processor reads stored frequency information from an adjacent memory into its internal memory, and sends the applicable receive frequency divisor (selected by the Channel switch) to the synthesiser on the Transceiver Board. It then sets the unit into standby mode and awaits a transmit command or a received message.

Standby Mode

4 When the unit is switched-on but is not actually transmitting or receiving a message, to save battery power, the processor switches-off the transmit circuits, and switches power to only the parts of the receive circuits that are required to detect the presence of an incoming message. While in the standby mode, the processor monitors the battery supply, and it provides an audible warning signal if power is low.

Transmit Secure

5 When the processor receives a PTT signal (i.e. a low signal of more than 1 ms duration on the PTT line), and the unit is set for secure operation, it switches power to the transmit and crypto circuits. It loads the transmit frequency divisor into the synthesiser, starts its transmit timer, illuminates the Transmit indicator and sets the crypto to transmit mode. The crypto outputs the preamble that is necessary for the receiving unit to synchronise, onto the transmit route.

6 The MIC input for transmission goes to the Crypto Board, where it is amplified to a constant level by a voice-operated gain adjusting device. The amplified signal goes via a bandpass filter to a codec module which converts it to the digital data form required by the crypto module. The crypto module encrypts the data using a keystream based on a stored cipher code (key variable), and starts to output encrypted data after the preamble. A transversal filter converts the squarewave data into a rounded-off form, TX SIG, that is more suitable for transmission.

7 TX SIG goes to the transmit buffer amplifer on the Control Board. The processor selects the gain of the amp so that the TX MOD level is optimised for the transmit frequency that is in use. TX MOD is amplified on the Transceiver Board then it modulates the frequency produced by the synthesiser. The synthesiser is a phase-locked loop in which the frequency of a voltage-controlled oscillator (VCO) is divided by a number (the divisor, sent by the processor) and compared with a reference frequency. The result of the comparison is a voltage which is used to drive the VCO faster or slower, as applicable, until the loop is balanced (in-lock) at the required transmit frequency.

8 The TX MOD signal modulates both the reference and the control voltage to the VCO: the output from the VCO is a frequency-modulated version of the original audio signal. This is amplified to RF levels by a three-stage power amplifier, filtered to remove harmonics, and the resulting RF I/O signal goes to the antenna.

Transmit Clear

9 When the processor receives a PTT signal and the unit is set for clear operation, operation is similar to secure transmission except the processor switches the MIC signal directly from the audio amplifier on the Crypto Board to the Control Board (i.e it bypasses the encryption circuits), and the processor adds a 150 Hz squelch tone to the input to the transmit modulation buffer amplifier. The processor also generates a slow-pip warning tone which it puts into the receive audio route to warn the operator that the transmission is not secure.

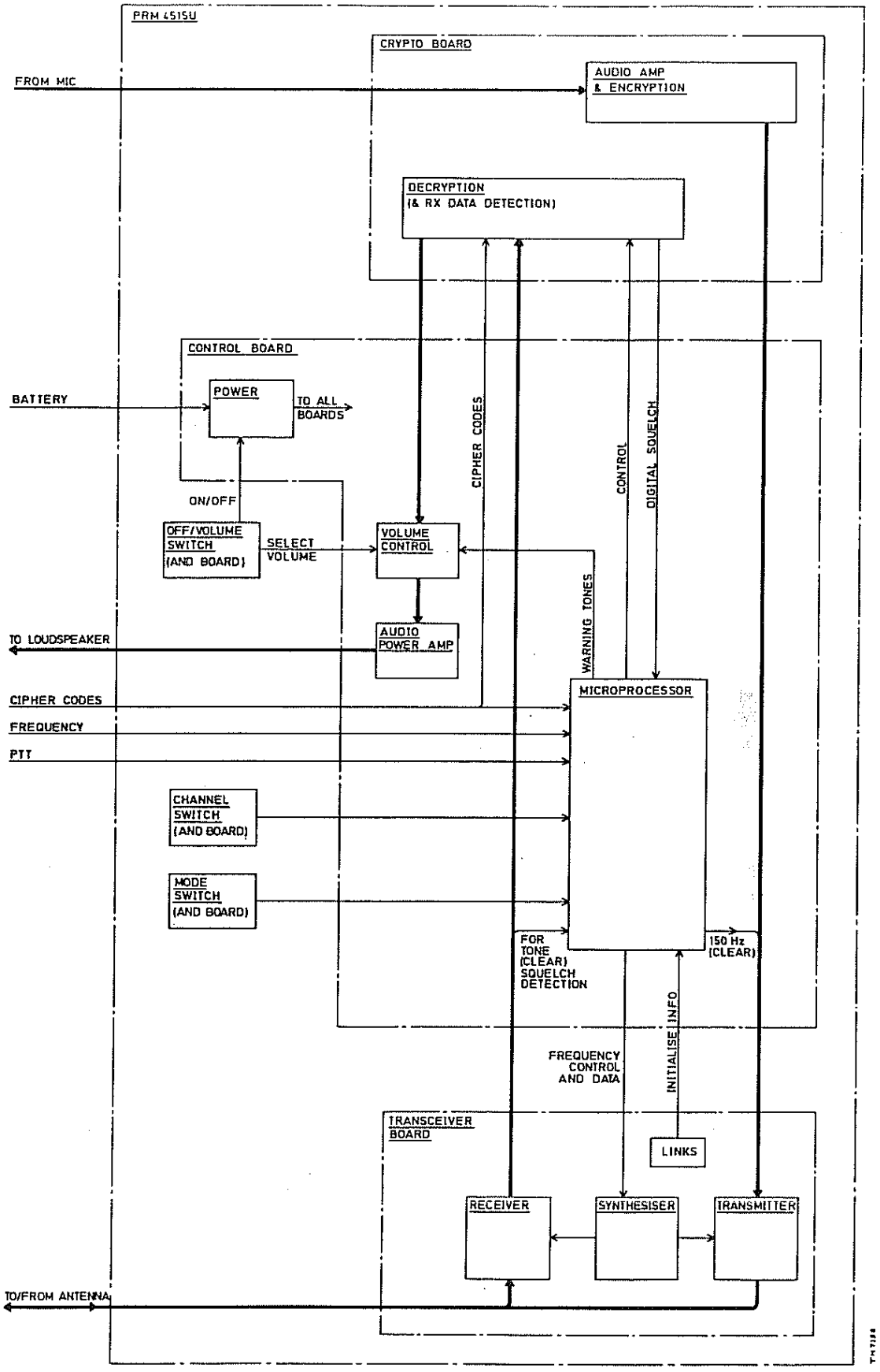


Fig 3.1 PRM4515U: Block Diagram

Transmit Wideband (Clear Data)

10 When the processor receives a PTT signal and the WIB input is active, it switches the MIC signal straight through the Crypto Board to the Control Board (i.e. it bypasses the audio amplifier and encryption circuits).

Receive Secure

11 When the unit is not transmitting, signals from the antenna go to the receiver circuits on the Transceiver Board. The received signal, filtered and amplified, goes to the first mixer, which has a local oscillator input provided by the synthesiser. A filter removes all mixer products except the modulated intermediate frequency (21.4 MHz) output, and this is amplified by the first IF amplifier. The second mixer, using a fixed crystal input, produces a modulated 455 kHz signal, which is clipped to a constant amplitude for use by the demodulator. This is a discriminator which produces a voltage that depends on the phase shift of the incoming signal (compared with the phase of a delayed version of the signal). The voltage therefore changes as frequency changes and thus it provides a demodulated version of the FM signal.

12 The recovered signal RX SIG goes via the Control Board to the Crypto Board. A slicer converts it into a squarewave, from which a 16k bit/sec detector detects the presence of 16k bit/sec data and produces a DSQ signal to inform the processor and crypto. The processor activates the crypto and the audio filter and amplifier. The clock recovery circuit produces a data bit rate clock that is in phase with the centre of the incoming data bits and supplies this to the crypto. The crypto uses the received sync code to set its decryption circuit, and check bits in the code enable the crypto to confirm that it is using the correct cipher code. The crypto then demutes the codec and decrypts the message. The codec converts the crypto's digital output to an analogue signal, RX Audio, which goes via the audio bandpass filter to the Control Board. The volume control circuit on the Control Board switches the audio signal through one of eight attenuating resistors, as selected by the inputs from the OFF/Volume switch, and the result is amplified to loudspeaker levels by the audio power amplifier.

Receive Clear

13 Clear signals are received in the same way as secure signals until RX SIG reaches the Control Board. Here the 150 Hz squelch tone is detected by the processor, which switches the received signal directly to the audio filter (i.e. it bypasses the decryption circuits).

Receive Wideband (Clear Data)

14 When the WIB input is active, the processor switches the received signal straight through the Crypto Board to the audio power amplifier on the Control Board (i.e. it bypasses the decryption circuits, audio filter and volume control circuits).

Receive Squelch-Open (Noise-On)

15 When the OFF/Volume switch is set to a Squelch-Open position, the processor routes the received signal continuously through the clear receive route (unless a 16k bit/sec signal is detected).

Warning Tones

16 The processor generates any required warning tones and routes them onto the receive route via the volume control circuit and audio power amplifier. If Squelch-Open is selected, the processor overrides this command when it has a warning tone to output.

Frequency, Cipher Code and Control Data

17 Data enters the unit via the PTT line, and interrupts the processor. The processor recognises the signal as data unless the level remains continuously low for 1 ms, in which case it recognises PTT. The processor decodes the 'header' at the start of the data to determine the data type. On receipt of frequency data, the processor calculates the divisor that will be needed by the synthesiser to produce the new frequency, and stores the divisor against the applicable transmit or receive channel number. On receipt of a cipher code header, the processor loads the subsequent cipher code data straight into the crypto. On receipt of data to control the unit's operating mode (clear/secure, squelch-open/normal, channel number, use of crypto key A or B, delete stored keys) the processor actions the command in the same way as it carries-out commands from the unit's own operator controls. To acknowledge receipt of data (except cipher codes), the processor echoes it back to the source.

OVERALL PERFORMANCE CHECKS

18 The performance checks can be carried out without dismantling the unit. If the unit is dismantled while the tests are carried out (e.g. after fault rectification), do not make random adjustments.

List of Test Equipment

19 (1) DC Power Supply

Voltage	:	10 V
Current	:	1A
Example	:	Farnell LT 30-2

(2) RF Power Meter

Frequency	:	500 MHz
Power	:	3 W
Impedance	:	50 ohm
Example	:	Hewlett Packard 436A

(3) Digital Frequency Meter

Frequency	:	500 MHz
Accuracy	:	Better than +/- 1 part in 10^7
Example	:	Racal 9917A option 04A

(4) Modulation Meter

Frequency	:	500 MHz
Deviation	:	Up to 10 kHz
Impedance	:	50 ohm
Filter	:	150 Hz notch
Example	:	Racal 9008M

(5) AF Signal Generator (two-tone)

Frequency	:	10 Hz to 10 kHz
Output	:	0 to 5 V rms (balanced)
Example	:	Racal 9083

(6) Audio Distortion Analyser/Voltmeter

Frequency	:	10 Hz to 20 kHz
Example	:	Hewlett Packard 339A

(7) RF Signal Generator

Frequency	:	500 MHz
Impedance	:	50 ohm
Output Level	:	-140 dBm to +13 dBm
Preferred Type	:	Hewlett Packard 8640B

(8) Multimeter (Two required)

Ranges	:	1 A, 10 V
Example	:	Racal 4002

(9) Test Aids

Audio Interface Jig (41117-100-10) BCC TJ 1117
RF Attenuator 50 ohm. 3 W. 500 MHz, 20 dB

(10) Ancillaries

Handset, 712433
Battery, MA4516A
Antenna, 29280-050-10 or 29280-051-10
Fill Gun, MA4083B

Setting-Up

20 (1) Connect PL1 of TJ1117 to the AUDIO Socket SK2 on the unit under test (UUT). Switch the TJ1117 to RX.

(2) Connect battery adaptor TJ2017 to the base of the UUT. Connect a power supply set to 9.7 V to the +V and 0V connections of the battery adaptor, with a multimeter, set to the 1 A range, in series. Ensure correct polarity. (See Figs. 3.3 and 3.4).

Programming

21 (1) Program channels 0 to 9 with the following Transmit/Receive frequencies using an MA4083B Fill Gun. (Connect the MA4083B to SK1 on TJ1117 and set the OFF/Volume switch on the UUT to an ON position).

Ch0	F0 + 0.075	MHz	Ch5	F0 + 11.1875	MHz
Ch1	F0 + 2.300	MHz	Ch6	F0 + 12.4125	MHz
Ch2	F0 + 4.525	MHz	Ch7	F0 + 15.6250	MHz
Ch3	F0 + 6.700	MHz	Ch8	F0 + 17.850	MHz
Ch4	F0 + 8.950	MHz	Ch9	F0 + 19.9125	MHz

F0 is the lowest frequency used by the UUT, and this is indicated by letter code (shown after 'PRM4515U' on the nameplate) as follows:

A - 403 MHz	D - 415	G - 427	K - 439
B - 407 MHz	E - 419	H - 431	L - 443
C - 411 MHz	F - 423	J - 435	M - 447
			N - 451

Transmitter Tests (Fig. 3.3)

22 (1) Connect a short coaxial lead from the ANTENNA socket SK1 on the UUT to the RF Power Meter. Select the 3 W range on the Power Meter.

(2) Select volume position 5 and channel 0 on the UUT.

(3) Switch TJ1117 to TX and adjust the Power Supply to give 9.7 V, measured at the connections to the radio. Check that the supply current is less than 700 mA.

(4) Check that the power output is greater than 1.3 W. Repeat for the channels 5 and 9.

(5) Connect the Frequency Meter to the UUT via the 20 dB attentuator. Check that the frequency is within ±5 ppm of nominal (approx ±2200 Hz).

(6) Disconnect the Frequency Meter and connect the Modulation Meter to the output of the Attenuator.

(7) Switch-out the 150 Hz Filter on the Modulation Meter. Switch TJ1117 to NB (Narrow Band). Select channel 2 and check that the deviation is between 0.5 kHz and 1.0 kHz.

(8) Connect the balanced output of the AF Signal Generator to terminals A and B on TJ1117 and set the Generator output to 10 mV at 1 kHz. Switch-in the 150 Hz Notch Filter on the Modulation Meter.

(9) Select channel 0 and check that the deviation is between 2.5 kHz and 4.0 kHz. Repeat for channels 5 and 9.

(10) Select channel 2. Reduce the level of the AF Signal Generator to give 3.0 kHz deviation. Check that the level is between 0.5 mV and 1.4 mV.

(11) Reduce the frequency of the AF Signal Generator to 400 Hz and check that the deviation is greater than 1.2 kHz.

(12) Increase the frequency of the AF Signal Generator to 2.5 kHz and check that the deviation is greater than 1.2 kHz.

(13) Set the OFF/Volume switch on the UUT to position 1. Set the frequency of the AF Signal Generator to 1 kHz and reduce the level to give 2.4 kHz deviation. Check that the level is between 0.12 mV and 0.40 mV.

(14) Switch TJ1117 to FLA mode. Adjust the AF Signal Generator level to give 2.4 kHz deviation. Check that the level is between 5 mV and 14 mV.

(15) Switch TJ1117 to WB (Wide Band) and switch out the 150 Hz Notch Filter on the Modulation Meter.

(16) Set the frequency of the AF Signal Generator to 1 kHz and increase the level to give 5 kHz deviation. Check that the level is between 0.36 V and 0.75 V.

(17) Increase the frequency of the AF Signal Generator to 10 kHz, and check that the deviation is greater than 2.5 kHz.

(18) Decrease the frequency of the AF Signal Generator to 30 Hz, and check that the deviation is greater than 2.5 kHz.

(19) If the UUT is fitted with an encryption module, set the Mode switch to A. (If the UUT has no cipher codes it produces a crypto alarm tone: load cipher codes). Check that the deviation is between 4.0 kHz and 6.0 kHz.

(20) Measure DC voltage across terminals C and E on TJ1117, with the multimeter. Check that this voltage is between 9 V and 10 V.

(21) Switch TJ1117 to RX, disconnect the AF Signal Generator from TJ1117, and disconnect the Attentuator from the ANTENNA socket SK1 on the UUT.

Receiver Tests (Fig. 3.4)

23 (1) Set the OFF/Volume switch on the UUT to position 7, 300 Ω/8 Ω switch to 300 Ω, and check that the supply current is less than 60 mA.

(2) Connect a handset to the 7-way socket on TJ1117, and check that noise is heard in the handset (squelch override).

(3) Disconnect the handset and set the OFF/Volume switch on the UUT to position 4. Check that the supply current is less than 50 mA.

(4) Connect a coaxial lead from the ANTENNA socket SK1 on the UUT to the RF Signal Generator. Set the radio to channel 0. Set the RF Signal Generator to the appropriate frequency, with a frequency modulated signal of 1 kHz at 4.0 kHz deviation; plus 150 Hz at 750 Hz deviation using the AF Signal Generator. Set the output level to -115 dBm.

(5) Connect the Audio Distortion Analyser to terminals D and E on TJ1117 and check that the SINAD is greater than 12 dB. Switch off the carrier of the RF Signal Generator and ensure that the audio output of the unit is muted. Repeat for channels 5 and 9.

(6) Increase the level of the RF Signal Generator to -60 dBm. Set modulation to 1 kHz at 4 kHz deviation. Switch TJ1117 to WB (Wide Band). Check that the audio output of the UUT is between 1.00 V and 2.0 V rms.

(7) Reduce the modulating frequency of the RF Signal Generator to 30 Hz and check that the audio output does not fall by more than 6 dB relative to 1 kHz.

(8) Increase the modulating frequency of the RF Signal Generator to 8 kHz and check that the audio level does not fall by more than 6 dB relative to 1 kHz.

(9) Connect the Multimeter between terminals G and E on TJ1117. Check that the voltage is between 4.0 V and 5.5 V.

(10) Switch off the carrier of the RF Generator and check that the voltage at terminal G is less than 0.1 V.

(11) Set the RF Signal Generator to -115 dBm with frequency modulation of 4.000 kHz ±2 Hz at 4.0 kHz deviation. Check that the voltage is between 4.0 and 5.5 V.

(12) Switch TJ1117 to NB (Narrow Band) and set the RF Signal Generator as in Para. 23(4). Switch on the carrier of the Generator.

(13) Set the OFF/Volume switch on the UUT to position 6 (highest noise-off volume).

(14) Switch in 8.2 Ω load on TJ1117. Check that the audio output of the UUT is greater than 1.7 V r.m.s. (Pins D and E of TJ1117).

(15) Switch out the 8.2 Ω load on TJ1117, and check that the audio output is greater than 1.7 V r.m.s.

(16) Set the OFF/Volume switch on the UUT to position 5. Check that the audio output is reduced by 4 +/- 3 dB compared with the level in Para 23(15).

(17) Set the OFF/Volume switch to position 4. Check that the audio output is reduced by 6 +/- 3 dB compared with the level in Para 23(16).

(18) Set the OFF/Volume switch to position 3. Check that the audio output is reduced by 6 +/- 3 dB compared with the level in Para 23(17).

(19) Set the OFF/Volume switch to position 2. Check that the audio output is reduced by 6 ±3 dB compared with the level in Para 23(18).

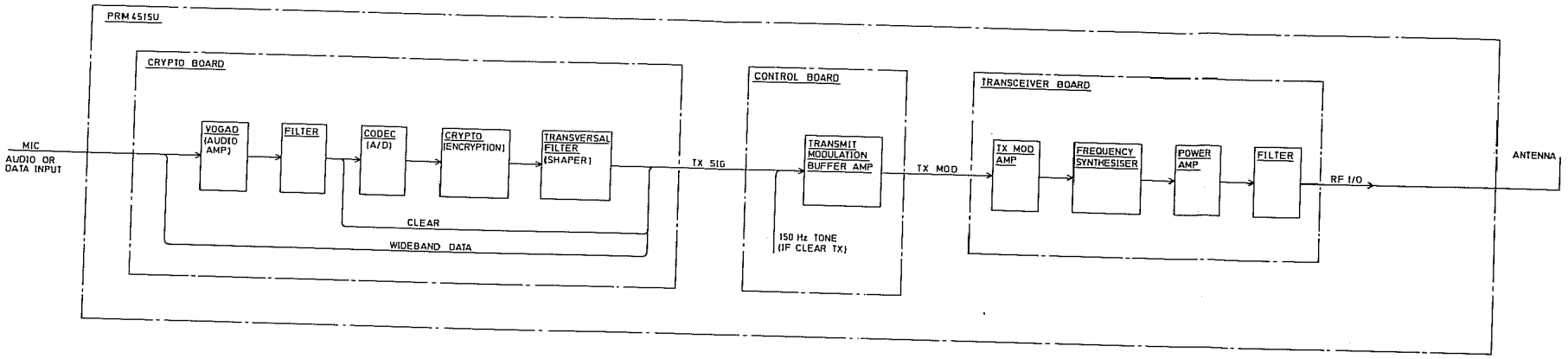
(20) Set the OFF/Volume switch to position 1. Check that the audio output is reduced by 6 ±3 dB compared with the level in Para 23(19).

(21) Reduce the modulating frequency of the RF Signal Generator to 400 Hz and check that the audio level does not fall by more than 6 dB relative to 1 kHz.

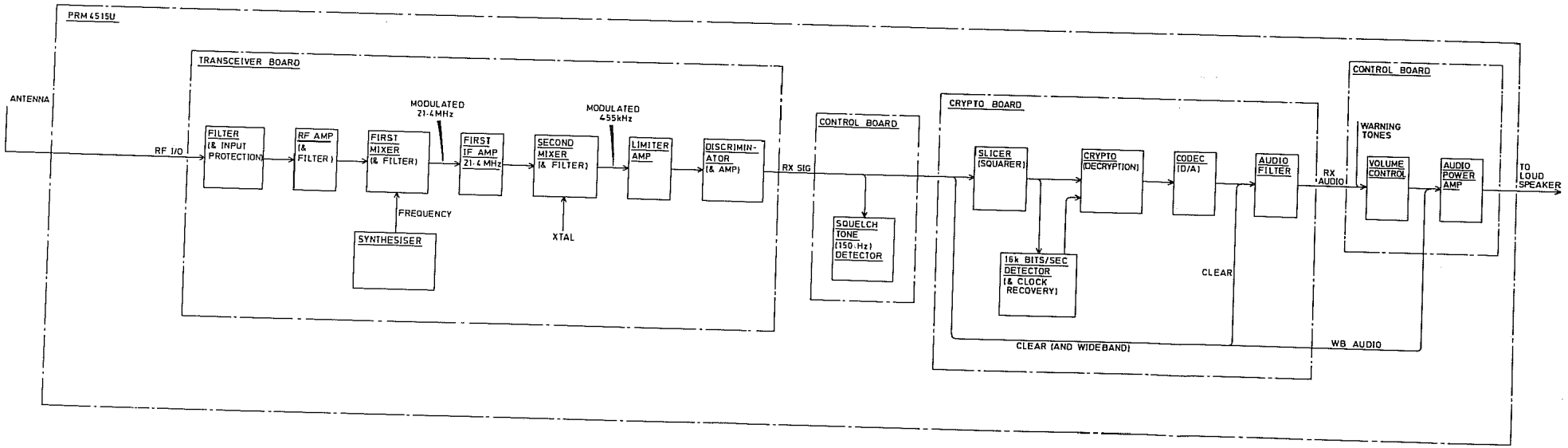
(22) Increase the modulating frequency of the RF Signal Generator to 2.5 kHz and check that the audio level does not fall by more than 6 dB relative to 1 kHz.

(23) Set the modulating frequency of the RF Signal Generator to 1 kHz and set the OFF/Volume switch to position 4.

(24) Switch TJ1117 to FLA and check that the audio output is between 1.50 V and 2.20 V r.m.s.



Route of Transmit Signal



Route of Receive Signal

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TX and RX Signal Routeing

Fig.3.2

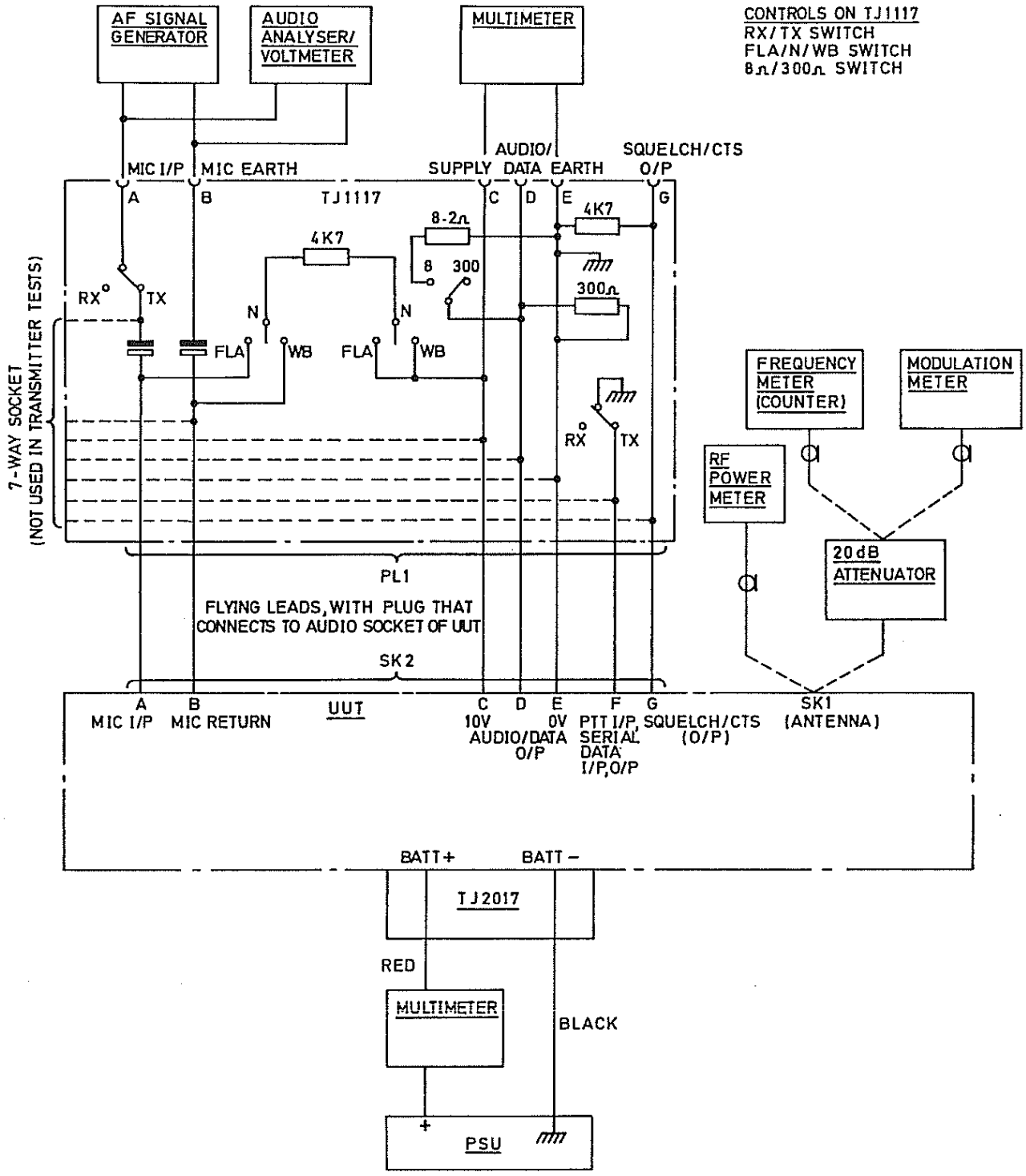
APPENDIX 1

PERFORMANCE CHECK LIST

Para.	Test		Upper Limit	Lower Limit	Result
	TRANSMITTER TESTS				
22(3)	Current		700 mA		
22(4)	Power Output	Chan 0		1.3 W	
		Chan 5		1.3 W	
		Chan 9		1.3 W	
22(5)	Frequency		5 ppm	5 ppm	
22(7)	Pilot Deviation		1.0 kHz	0.5 kHz	
22(9)	1 kHz Deviation	Chan 0	4.0 kHz	2.5 kHz	
		Chan 5	4.0 kHz	2.5 kHz	
		Chan 9	4.0 kHz	2.5 kHz	
22(10)	Modulation Sensitivity NB		1.4 mV	0.5 mV	
22(11)	Bandwidth NB 400 Hz			1.2 kHz	
22(12)	Bandwidth NB 2.5 kHz			1.2 kHz	
22(13)	Modulation Sensitivity NB Whisper		0.40 mV	0.12 mV	
22(14)	Modulation Sensitivity NB FLA		14 mV	5.0 mV	
22(16)	Modulation Sensitivity WB		0.75 V	0.36 V	
22(17)	Bandwidth WB 10 kHz			2.5 kHz	
22(18)	Bandwidth WB 30 Hz			2.5 kHz	
22(19)	Secure deviation		6.0 kHz	4.0 kHz	
22(20)	Pin C DC Voltage		10.0 V	9.0 V	
	RECEIVER TESTS				
23(1)	Current receiving		60 mA		
23(2)	Noise (squelch overide)		*	*	
23(3)	Current economise		50 mA		
23(5)	SINAD	Chan 0		12 dB	
		Chan 5		12 dB	
		Chan 9		12 dB	
	Squelch	Chan 0	*	*	
		Chan 5	*	*	
		Chan 9	*	*	
23(6)	Output WB		2.00 V	1.50 V	
23(7)	Bandwidth WB 30 Hz		-6 dB		
23(8)	Bandwidth WB 8 kHz		-6 dB		

Para.	Test	Upper Limit	Lower Limit	Result
23(9)	CTS	5.5 V	4.0 V	
23(10)	CTS	0.1 V	0 V	
23(11)	CTS (Secure)	5.5V	4.0 V	
23(14)	Output NB		1.7 V rms	
23(15)	Output NB Vol 6		1.7 V rms	
23(16)	Output NB Vol 5	-1 dB	-7 dB	
23(17)	Output NB Vol 4	-3 dB	-9 dB	
23(18)	Output NB Vol 3	-3 dB	-9 dB	
23(19)	Output NB Vol 2	-3 dB	-9 dB	
23(20)	Output NB Vol 1	-3 dB	-9 dB	
23(21)	Bandwidth NB 400 Hz	-6 dB		
23(22)	Bandwidth NB 2.5 kHz	-6 dB		
23(23)	Output FLA	2.2 V rms	1.5 V rms	

* Record Result as Satisfactory or Unsatisfactory.



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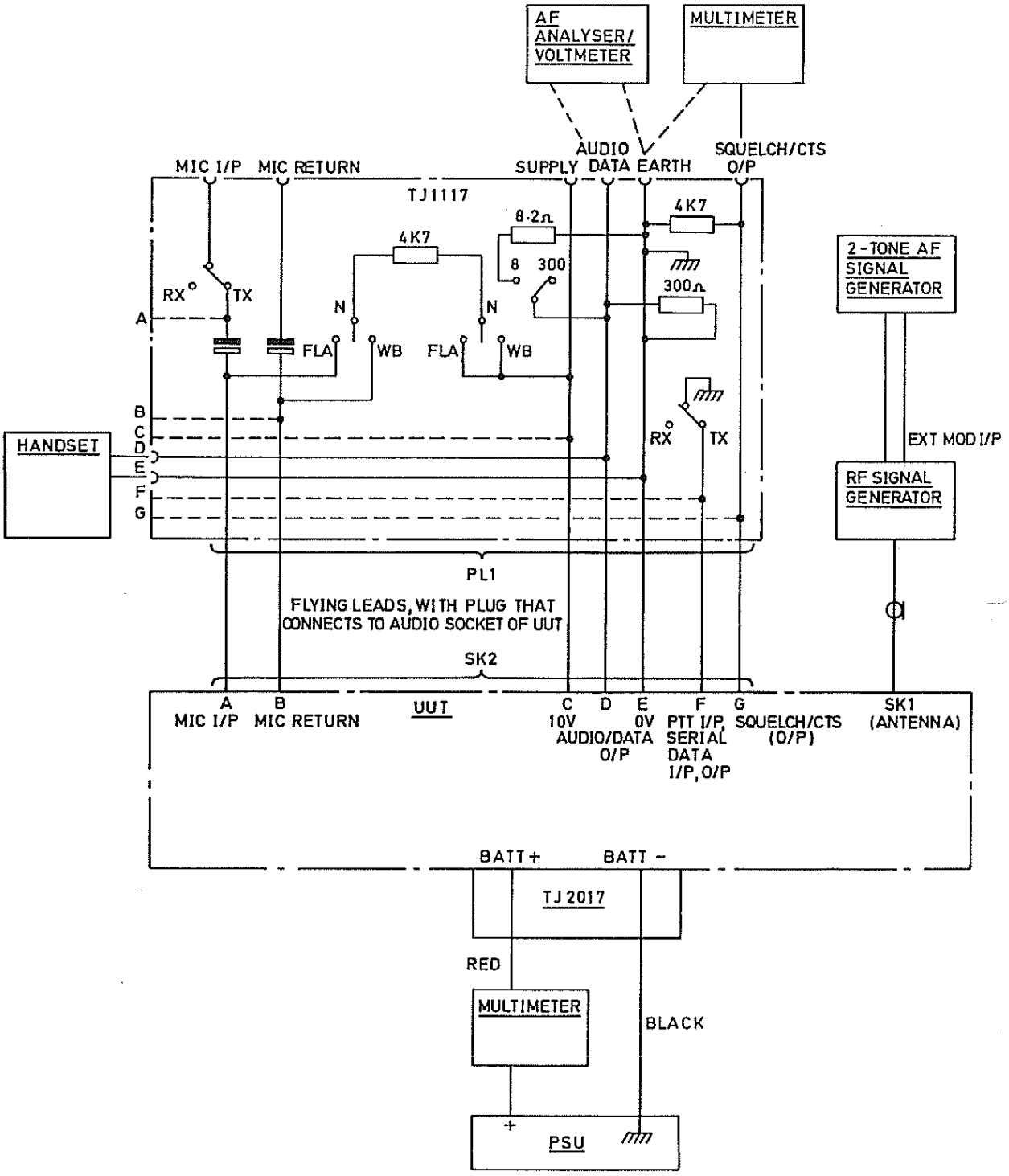
Test Equipment Configuration for Transmitter Tests

Fig.3.3



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Test Equipment Configuration for Receiver Tests

Fig.3.4

CHAPTER 4

TRANSCEIVER BOARD

CONTENTS

	Page
INTRODUCTION	4-1
BRIEF DESCRIPTION	4-1
Power and Tx/Rx Switching	4-1
Transmitting	4-1
Receiving	4-4
DETAILED DESCRIPTION	4-5
Transmit/Receive Switching and Power	4-5
TRANSMITTER	4-6
Tx Mod Amplifier	4-6
Reference Oscillator	4-6
TX VCO	4-7
Power Amplifier	4-8
Automatic Level Control (and Battery Voltage Monitor)	4-8
RECEIVER	4-9
Rx RF Amplifier	4-9
First Mixer, First IF Amp and RX VCO	4-9
Second Mixer, Second IF Amp and Demodulator	4-10
SYNTHESISER	4-11
Synthesiser IC	4-11
Prescaler	4-12
Current (Charge) Pump and Loop Filter	4-12
INITIALISE REGISTER (AND FREQUENCY-BAND SELECTION)	4-12
FUNCTIONAL TESTS AND ALIGNMENT	4-15
TYPICAL VOLTAGES AND WAVEFORMS	4-15
EQUIPMENT REQUIRED FOR TRANSCEIVER BOARD TESTS	4-15

TABLES

Table No.

1	Initalisation Data
2	Frequency Band Selection
3	Timeout Selection
4	Interboard Connector Listing
5	Transmitter Alignment
6	Receiver Alignment
7	Static Reference Voltages

ILLUSTRATIONS

Fig. No.

4.1	Transmit Signal Routeing
4.2	Modulation and Synthesiser Principles
4.3	Transceiver Board: Block Diagram
4.4	Receive Signal Routeing
4.5	Transmit/Receive Switching
4.6	Tx Mod Amplifier and Reference Oscillator
4.7	TX VCO
4.8	Power Amplifier
4.9	Automatic Level Control (and Battery Voltage Monitor)
4.10	Rx RF Amplifier and RF Head
4.11	First Mixer and First IF Amplifier
4.12	Second Mixer, Second IF Amp and Demodulator
4.13	Synthesiser
4.14	Initialise Register
4.15	Transceiver Board: Circuit
4.16	Transceiver Board: Layout
4.17	Test Equipment Configuration for Transceiver Board Alignment

CHAPTER 4

TRANSCEIVER BOARD

INTRODUCTION

1 The Transceiver Board contains the transmitter and receiver circuits, and the frequency synthesiser.

BRIEF DESCRIPTION (Fig. 4.3, 4.5)

Power and Tx/Rx Switching

2 The board is powered by regulated 5VC and 8VC, which are present when the unit is switched on, and a direct 10V BATT battery input drives the power amplifier when the unit is transmitting. For a transmit operation, CTX switches 8VC and 10V Batt to the transmitter and removes power from the receiver. For receive, it removes power from the transmitter and allows 8VC to the receiver. 5VC powers the synthesiser during both transmit and receive operations.

Transmitting (Fig. 4.1, 4.2)

3 The TX MOD signal for transmission is amplified, then it modulates the output from the transmit voltage-controlled oscillator (TX VCO). The frequency modulated output from the TX VCO is amplified to radio frequency (RF) levels by the power amplifier (PA) and the output from the amplifier goes to the antenna, as RF I/O.

4 The basic output frequency of the TX VCO is set and held by a phase-locked loop. Feedback from the TX VCO goes to a synthesiser IC which divides it down by a preset number (entered at the start of

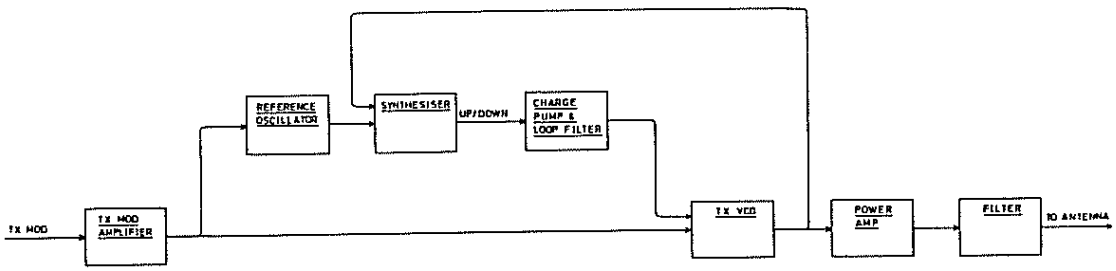


Fig 4.1: Transmit Signal Routeing

each transmit operation), and compares the result with a reference. If the two are the same, the TX VCO output is correct; the loop is in-lock. If the two differ, the synthesiser IC produces a Pump Up or a Pump Down output to increase or decrease the charge on a capacitor, and this, in turn, increases or decreases the voltage applied to the VCO and hence the VCO's output frequency.

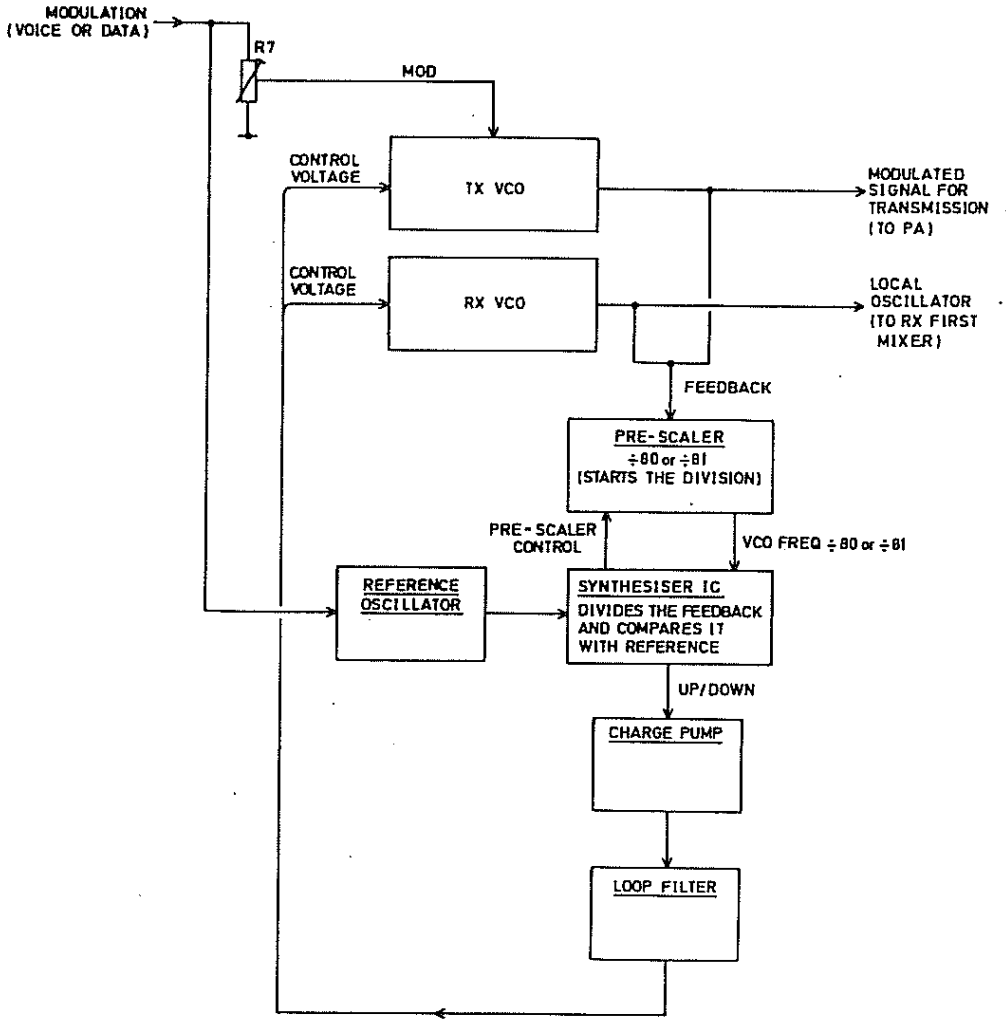


Fig 4.2 Modulation and Synthesiser Principles

5 To achieve the required wide modulation bandwidth, the TX MOD signal modulates both the reference and the VCO, with balance provided by a potentiometer. TX MOD modulates the reference frequency, so the VCO output is modulated as the loop adjusts to balance the changing reference; and TX MOD changes the VCO's control voltage directly, thus modulating the output. Because of the characteristics of the loop, direct VCO modulation is most effective above 1 kHz; at the lower frequencies the modulation of the reference is most effective. Therefore, the dual modulation produces an even response throughout the 10 Hz to 10 kHz voice and data bandwidth.

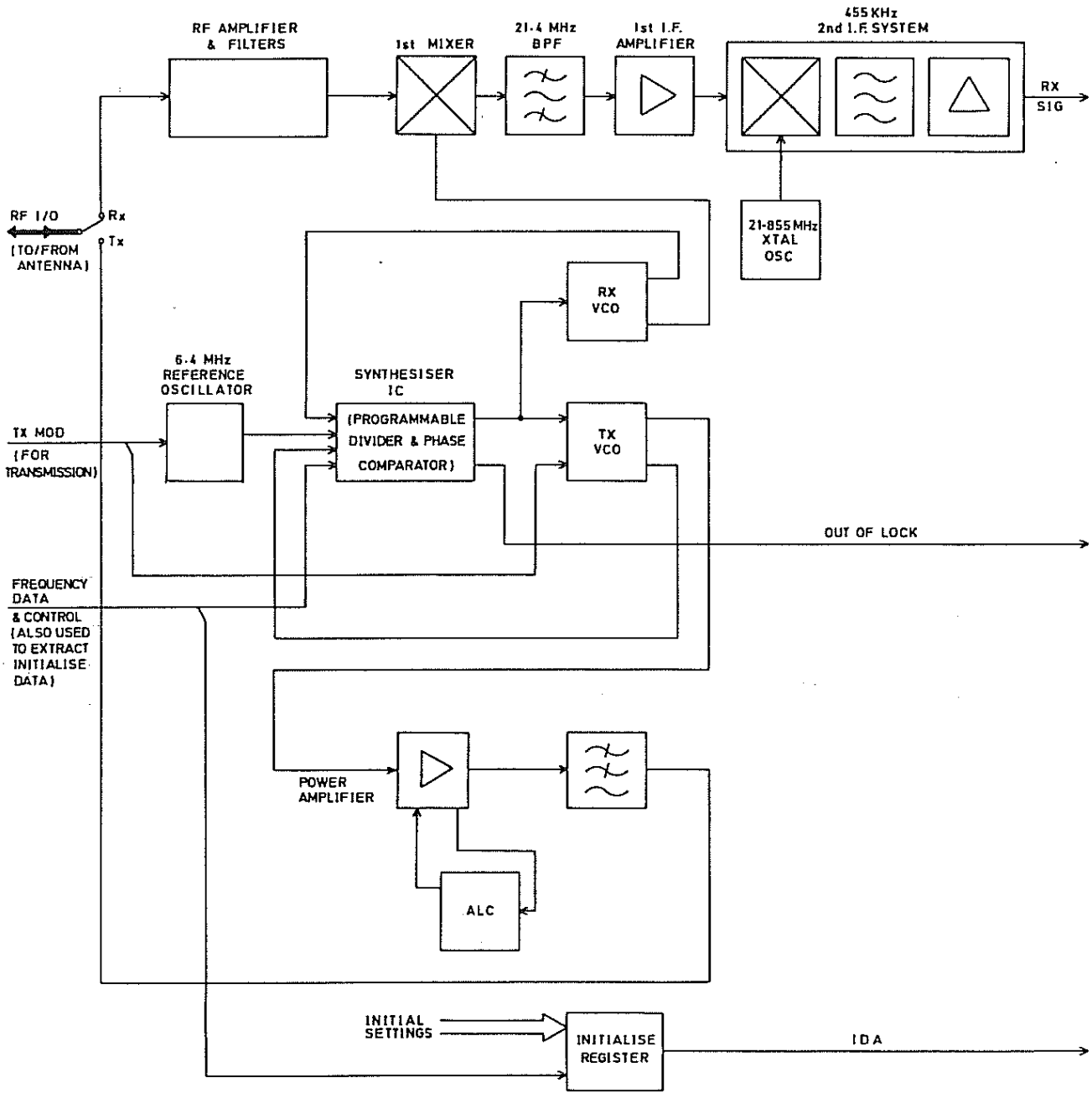


Fig 4.3 Transceiver Board: Block Diagram

6 If the synthesiser goes out of lock, it increases the current to charge/discharge the capacitor (Para. 4) in an attempt to regain lock, and produces a status signal to inform the (off-board) control processor.

7 The power amplifier consists of three stages: buffer (pre-driver), driver and final output. Automatic level control prevents the final output stage from drawing excessive current, by reducing the supply to the driver stage. Output filters remove harmonics and match the power amplifier to the antenna.

Receiving (Fig. 4.4)

8 The RF I/O received signal from the antenna, bandpass filtered, goes to the Rx RF amplifier, which converts it to levels suitable for the first intermediate frequency (IF) mixer. An input protection circuit prevents excessive signals from reaching the amplifier, and filters reject image frequencies.

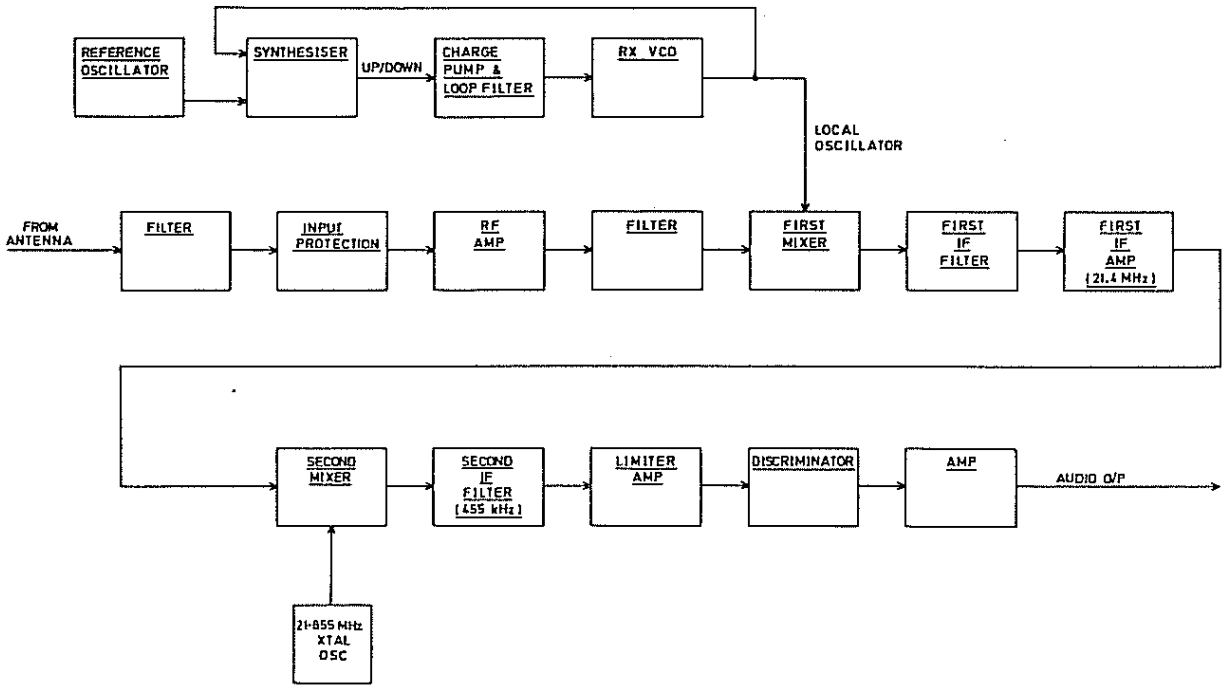


Fig 4.4 Receive Signal Routeing

9 The first IF mixer mixes the amplified signal with the local oscillator frequency produced by the RX VCO. The RX VCO is similar to the TX VCO (described previously), and it produces a frequency 21.4 MHz below that of the received signal. The mixing process results in a modulated first IF signal at 21.4 MHz. A filter removes the unwanted products of the mixer, then the signal is amplified by the first IF amplifier, tuned to 21.4 MHz.

10 The second IF mixer mixes the signal with 21.855 MHz from a crystal oscillator. The resulting modulated second IF signal at 455 kHz is filtered then a limiting amplifier clips it to a constant amplitude. A discriminator (quadrature detector) produces a voltage that depends on the frequency, and thus recovers the original audio signal. A filter removes the 455 kHz from the recovered audio signal, which is amplified and output as RX SIG.

DETAILED DESCRIPTION (Fig. 4.15)

Transmit/Receiver Switching (Fig 4.5)

11 For transmit, CTX (PL1/3) is high. This switches on FET TR26, so FET TR22 switches 8VC (PL1/10) as 8VTX to the Tx Mod amplifier (TR1 plus associated components), power amplifier and TX VCO. TR26 on allows FET TR25 to conduct so FET TR24 removes the 8VRX supply from the receiving circuits. FET TR25 switches 10V BATT (PL1/4) to the power amplifier.

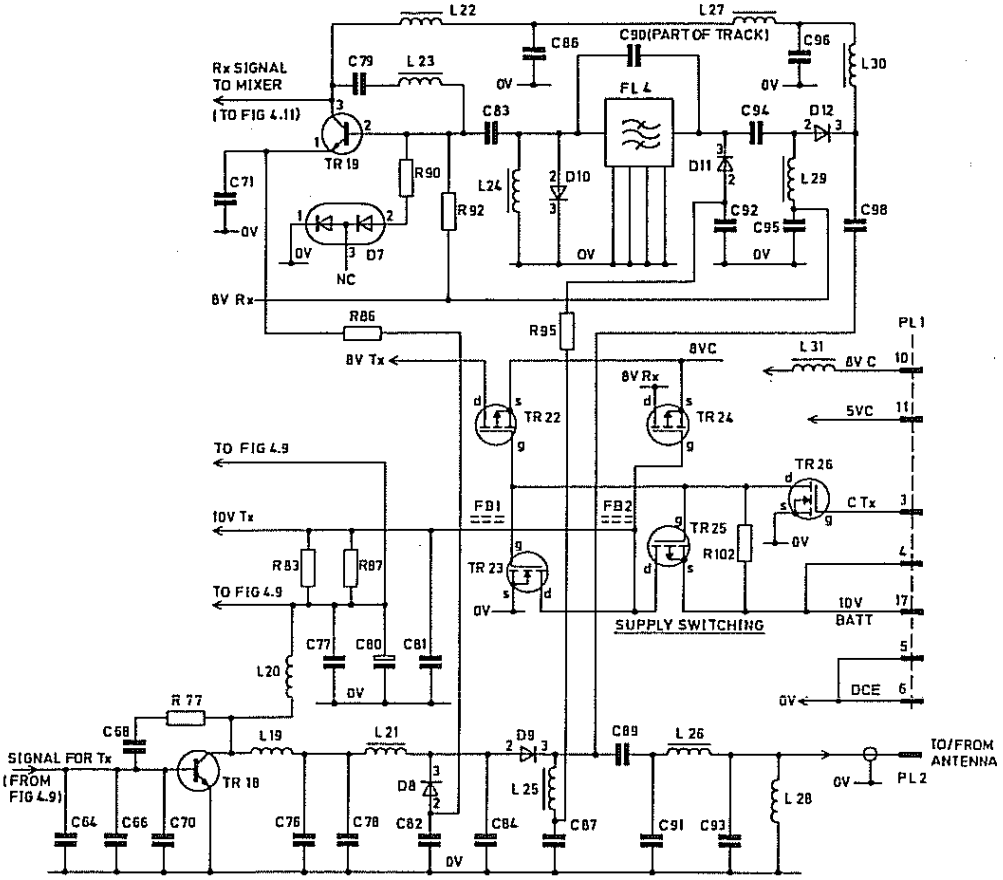


Fig 4.5 Transmit/Receive Switching

12 A system of diodes isolates the receive circuits during transmission and provides protection against excessive inputs. In receive, 8VRX provides current via diode D12, inductor L30, transistor TR19, and D8, onto the 10VTX line which is grounded by FET TR23. In transmit, the junction of TR18/R77/L19 is nominally 10V, which reverse biases D8 (no longer conducting). Current goes through D9, D11 and to ground via the input of filter FL4.

TRANSMITTER

Tx Mod Amplifier (Fig 4.6)

13 The TX MOD signal (PL1/20) for transmission goes to a broadband amplifier that consists of transistor TR1, plus associated components. The output from the amplifier modulates the reference oscillator and the TX VCO, with balance provided by potentiometer R7.

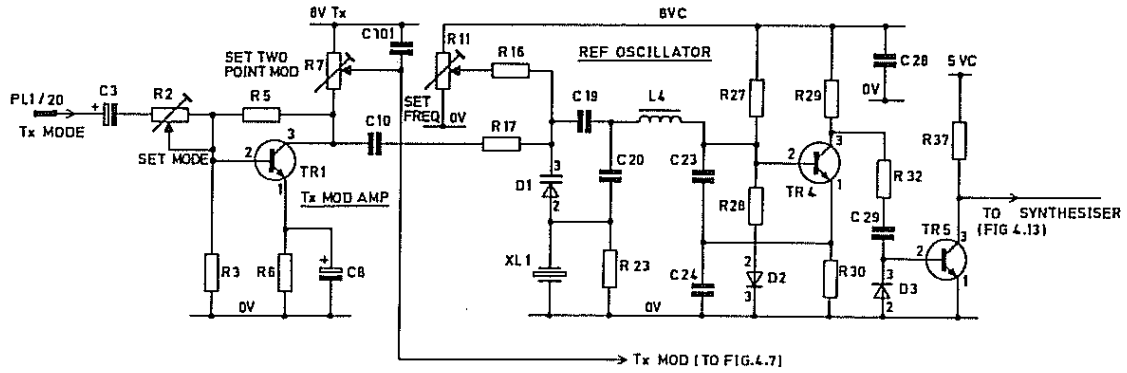


Fig 4.6 Tx Mod Amplifier and Reference Oscillator

Reference Oscillator (Fig 4.6)

14 The crystal-controlled oscillator based on crystal XL1 provides a 6.4 MHz reference clock signal for the synthesiser IC, IC3. The oscillator is tuned by varactor D1 which has a capacitance that varies with the applied voltage. The TX MOD amplified signal applied to the circuit therefore frequency modulates the output from the oscillator. Potentiometer R11 sets the mean frequency. Transistor TR5 squares-up the oscillator's output and switches it through to the synthesiser at logic levels.

TX VCO (Fig 4.7)

15 The TX VCO produces the transmit frequency, according to the voltage received from the synthesiser loop filter circuit. The voltage is modulated directly by TX MOD from potentiometer R7, and by changes to the loop filter output caused by TX MOD modulating the reference oscillator. Inductor 4cL1, varactor 4cD1 plus associated components produce oscillations at a frequency that depends on the applied voltage. Transistor 4cTR1 amplifies the signal. The output goes to the power amplifier for transmission, and as feedback to the synthesiser's prescaler.

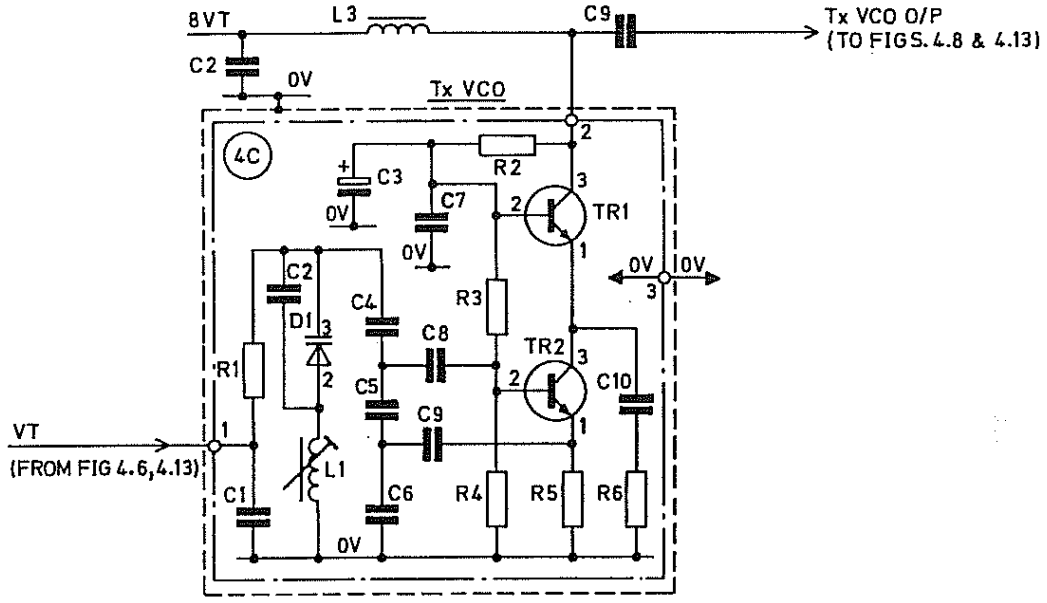


Fig 4.7 TX VCO

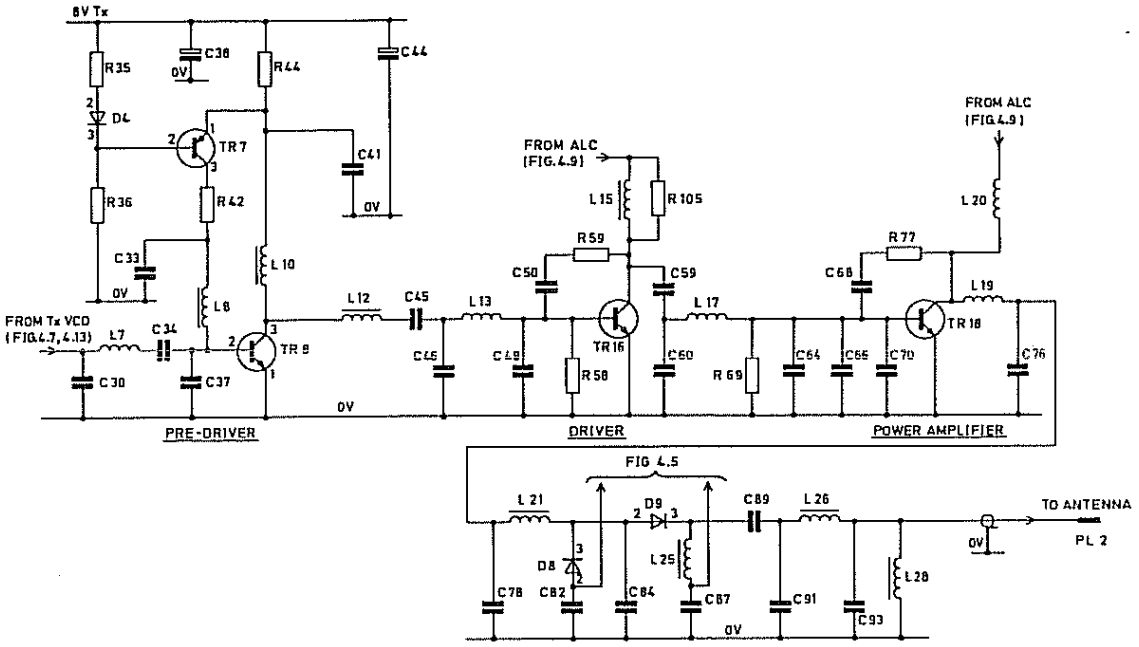


Fig 4.8 Power Amplifier

Power Amplifier (Fig 4.8)

16 The TX VCO output (about 1-2 mW) drives the pre-driver stage, transistor TR8 plus associated components, which raises the output to about 50 mW. The buffer's output goes via an impedance-matching and filtering network, L12, L13 plus associated components, to the class C amplifier driver stage. This is TR16 plus associated components, which raise the output to about 500 mW.

17 The driver's output goes via an impedance-matching and filtering network, L17 plus associated components, to the class C amplifier final stage, TR18. L19, L21, plus associated components attenuate harmonics, L26/C91/C93 provide additional low-pass filtering and L28 removes static and EMI (the L26 and L28 circuits are also used by received signals). The output, RF I/O, goes to the antenna via PL2.

Automatic Level Control (and Battery Voltage Monitor) (Fig 4.9)

18 The automatic level control circuit, op amp IC4b plus associated resistors, is a bridge network which controls the current to transistors TR16, TR18. The voltage across potentiometer R68 determines the current drawn from the battery supply: if excessive current is drawn the voltage across C80 reduces and the op amp's output (pin 7) goes low, so TR13, TR11 turn off and the dc to the driver stage (TR16) is reduced. Thermistor R81 provides thermal protection. It is located on the body of TR18, and shuts down the power amplifier if the temperature (of TR18) exceeds 120°C.

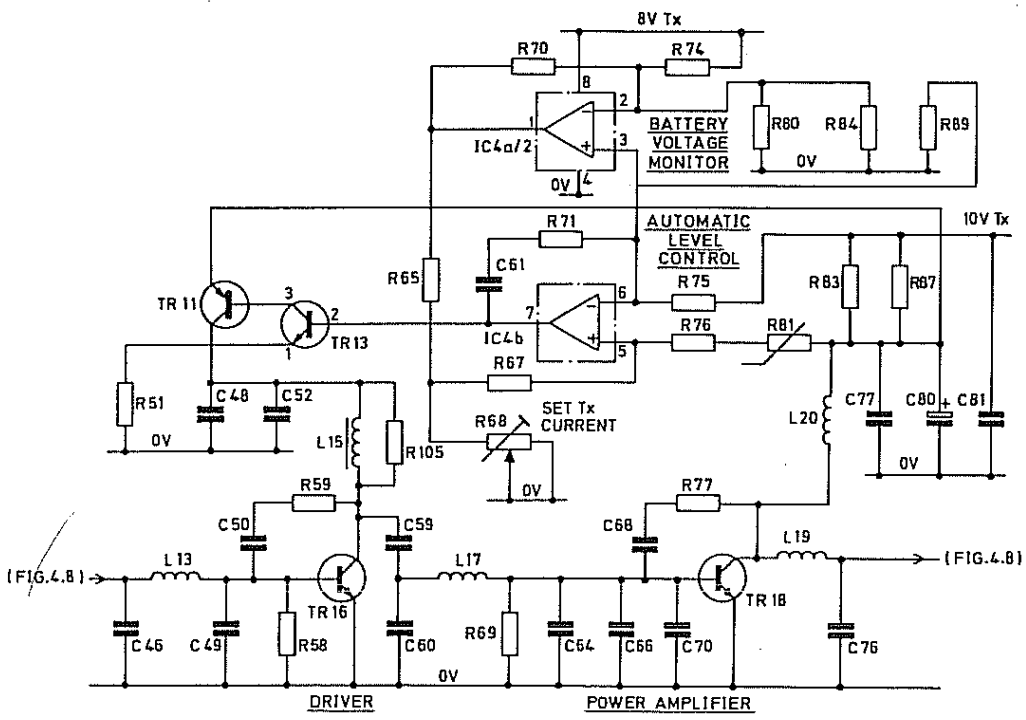


Fig 4.9 Automatic Level Control and Battery Voltage Monitor

19 The battery voltage monitor, op amp IC4a plus associated resistors, compares the battery voltage with the regulated 8VC supply. If the battery voltage falls below 8.6 V (approx), the op amp's output (pin 1) goes low, the voltage across R68 falls and op amp IC4b reduces the supply to the driver stage (as in Para. 18).

RECEIVER

Rx RF Amplifier (Fig 4.10)

20 The Rx RF Amplifier amplifies the received RF I/O signal (PL2) to levels suitable for use by the first IF mixer. Three-cavity helical filters FL4, FL3 plus associated capacitors attenuate image frequencies, and transistor TR19, which has a temperature-compensated bias provided by D7, amplifies the filtered signal. Note that the capacitance shown as C90 is provided by two parallel strips of track. (This applies also to C65). Transformer T1 matches TR19 to the input impedance of the next stage (FL3).

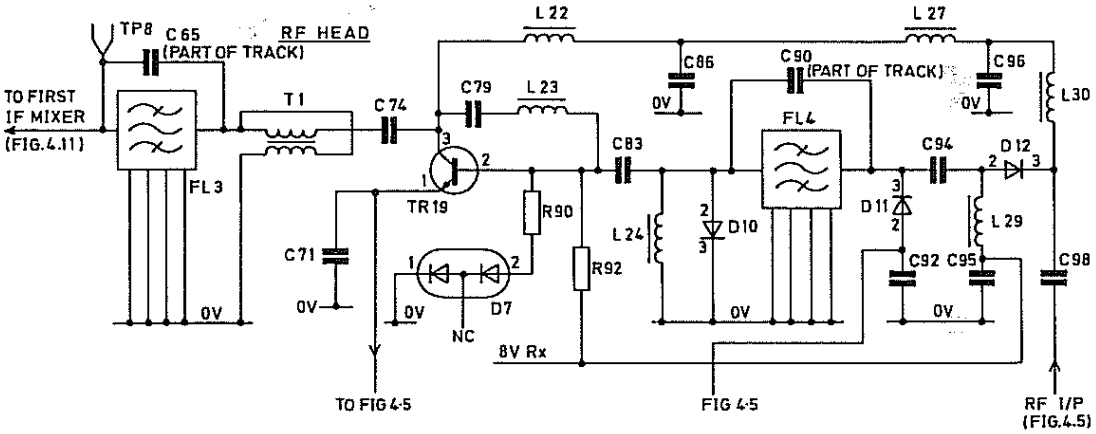


Fig 4.10 Rx RF Amplifier and RF Head

First Mixer, First IF Amp and RX VCO (Fig 4.11)

21 The output from the Rx RF amplifier goes via the three-cavity helical filter FL3, then mixer ML1 mixes it with the RX VCO (local oscillator) output, which is 21.4 MHz below the frequency of reception. The RX VCO operates in a similar way to the TX VCO (Para. 15). The resulting output from the mixer includes a

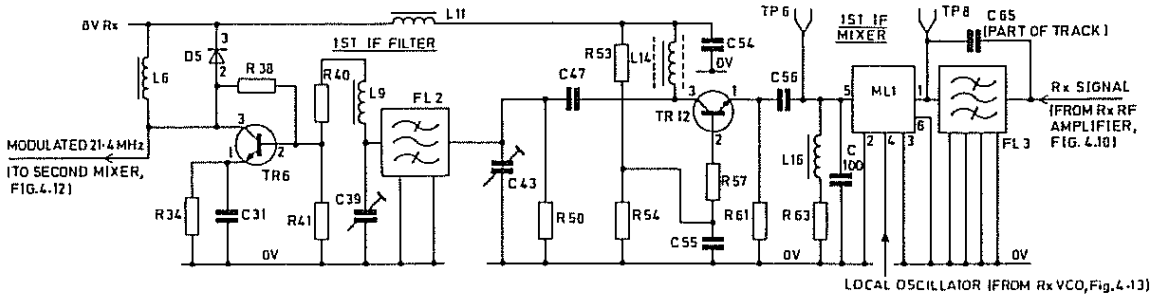


Fig 4.11 First Mixer and First IF Amplifier

modulated 21.4 MHz signal. Crystal filter FL1 removes the unwanted products of the mixing process, leaving the modulated 21.4 MHz signal. This is amplified by the first intermediate-frequency amplifier, transistor TR6 plus associated components, tuned to the 21.4 MHz IF frequency.

Second Mixer, Second IF Amp and Demodulator (Fig 4.12)

22 The output from the first mixer amplifier goes to the RF IN input (pin 16) of FM IF IC, IC1. This IC, with its associated components, provides second IF mixing, filtering, amplification and limiting, followed by detection of the modulating signal.

23 The IC mixes the 21.4 MHz signal with the 21.855 MHz signal produced by crystal oscillator XL2 (plus associated components). The result, from pin 3, is filtered by ceramic 455 kHz bandpass filter FL1 to provide a modulated 455 kHz signal. This goes, via pin 5, to a limiter amp, and the constant amplitude output from the limiter drives a discriminator, both directly (pin 7), and indirectly via a quadrature coil L1 (pin 8), which is tuned to phase-shift it by 90°. The discriminator detects phase changes: an advance (caused by a frequency decrease) results in an increased output voltage; a retardation (caused by a frequency increase) results in a decreased output voltage.

24 The recovered audio signal leaves the IC at pin 9. C14, R14 filter out any remaining 455 kHz in the signal. An inverting amplifier (pins 10, 11) provides additional audio buffering. The audio signal leaves the board as RX SIG (PL1/19).

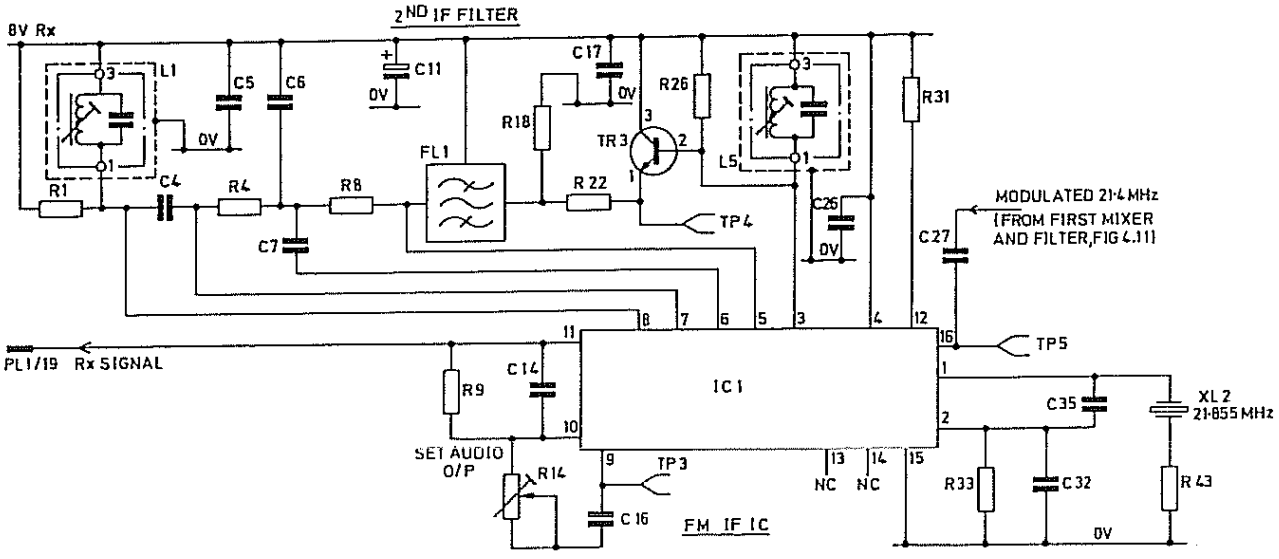


Fig 4.12 Second Mixer, Second IF Amp and Demodulator

SYNTHESISER (Fig 4.13)

Synthesiser IC

25 The synthesiser IC, IC3, has a variable counter which divides the frequency produced by the (applicable) VCO by a preset number (divisor). The number is chosen such that the result of the division is 12.5 kHz when the VCO is producing the required frequency. The synthesiser also divides the 6.4 MHz reference input to 12.5 kHz. It compares the phase and frequency of the two results and, if they are different, produces unequal duration Pump Up and Pump Down outputs to increase or reduce the frequency, as applicable. This is implemented as follows.

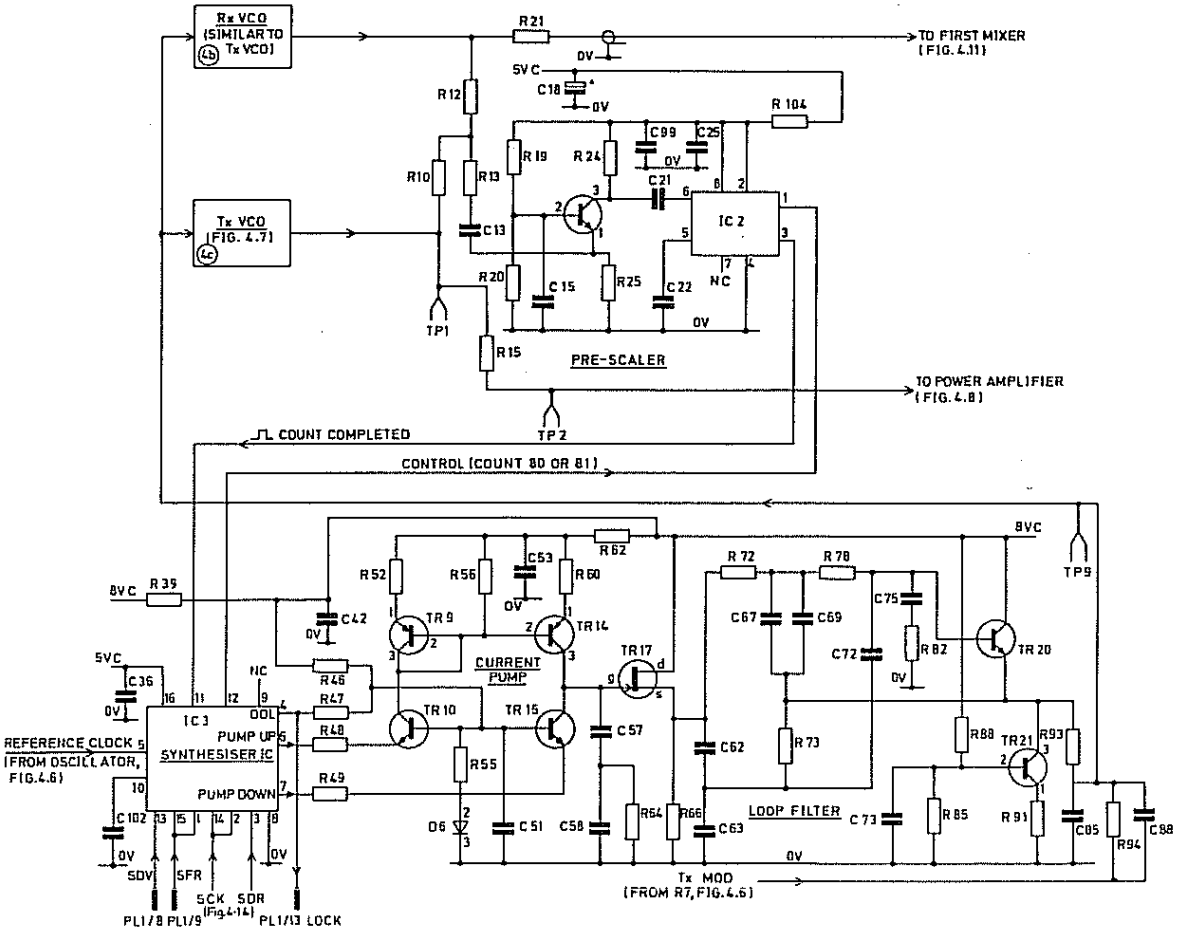


Fig 4.13 Synthesiser

26 When the frame signal (SFR, PL1/9, to pins 1 and 15 of IC3) is high, clock pulses (SCK, PL1/14, to pins 2 and 14) clock-in the divisor that presets the variable counter (SDV, PL1/8, to pin 13), and the divisor for the reference counter (SDR, PL1/12, to pin 3). The variable counter counts feedback pulses from the VCO (to pin 11).

The feedback has already been partly divided, by prescaler IC2, to a level that is suitable for use by IC3. The reference counter counts reference clock pulses (pin 5), and completes its count 12.5 k times per second. The two counts should be completed at the same time. If this occurs, IC3 produces two equal (and simultaneous) pulses, a low Pump Up pulse (pin 6) and a low Pump Down pulse (pin 7) to drive the current (charge) pump. If the feedback frequency is low, its end of count is late and IC3 makes Pump Up a longer pulse; if the feedback frequency is high, its end of count is early and IC3 makes Pump Down a longer pulse.

27 When the synthesiser loop is in lock (i.e. it is receiving the correct number of feedback pulses per sampling period), the Out Of Lock (OOL) signal from IC3 (pin 4) stays low. When the loop is out of lock, OOL high increases the voltage at the bases of TR10, TR15 to speed up the return to the lock condition. The OOL signal also leaves the board as a status signal (Lock, PL1/13).

Prescaler

28 The prescaler, IC2, is a variable-modulus counter: it counts either 80 or 81 of the pulses received at pin 6, depending on the setting of the Control input to pin 1. The pulses to pin 6 are either feedback from the RX VCO or TX VCO via TR2.

29 The MOD CONT output (pin 12) of synthesiser IC3 controls the 80/81 division ratio. The prescaler acts as the first part of IC3's programmable divider: it basically produces one pulse from pin 3 for every 80 VCO pulses received. To allow for frequencies that are not exact multiples of 80, the prescaler can count 81. If, for example the overall division needs to be by 24000, the counter counts 80 three hundred times; if the division is 24003 the counter counts 81 three times then it counts 80 two hundred and ninety seven times, thus it presents the correct number of pulses to IC3, for further division, during the sampling period.

Current (Charge) Pump and Loop Filter

30 The current (charge) pump is transistors TR9, TR10, TR14, TR15, connected such that a low Pump Up signal from IC3 charges capacitor C57 and a low Pump Down signal discharges the capacitor. The capacitor's charge represents the average of the 12.5 kHz sampling up/down results from IC3, and this drives FET TR17. The output from TR18 is smoothed by R72, R78 plus associated components, and drives buffer amplifier TR20, TR21 which provides the control voltage for the (applicable) VCO.

INITIALISE REGISTER (AND FREQUENCY-BAND SELECTION) (Fig 4.14)

31 The initialise register IC5 has eight parallel input signals, which are loaded into the register when P/S (pin 9) goes high. Clock pulses to pin 10 clock out the contents of the register, serially, in the order P8 to P1, via Q8 (pin 3), as IDA (PL1/18). The signals

are basic setting-up information that the (off-board) processor reads immediately after switch-on. It uses the SDR line to load the data into the register, then it sends pulses on the SCK line to clock the information out.

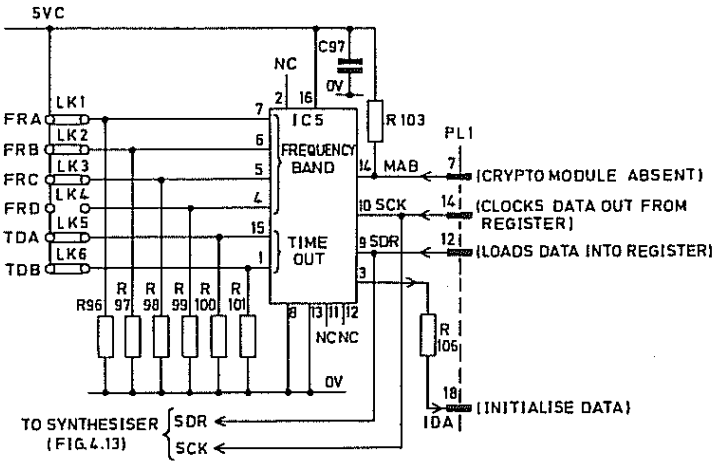


Fig 4.14 Initialise Register

32 Six of the inputs are set by links LK1 to LK6. A link is fitted to hold the corresponding input high (1); a link is not fitted for low (0). Note that in addition to the link changes (Table 2), a change of frequency band involves changing or resetting filters FL3, FL4 and the TXVCO and RXVCO. Resetting is possible between the groups of frequency bands connected by a thick black line (in the Table). In some cases, other settings and component value changes may also be necessary.

TABLE 1

Initialisation Data

Input	Pin	Signal
P1 (FRA, LK1)	7	) Define the 20 MHz band in
P2 (FRB, LK2)	6	) which the Transceiver Board
P3 (FRC, LK3)	5	) operates (see Table 2).
P4 (FRD, LK4)	4	)
P5	13	Held low to indicate UHF operation.
P6	14	MAB (Crypto Module Absent).
P7 (TDA, LK5)	15	) Select Timeout
P8 (TDA, LK5)	1	) (see Table 3).

TABLE 2

Frequency Band Selection

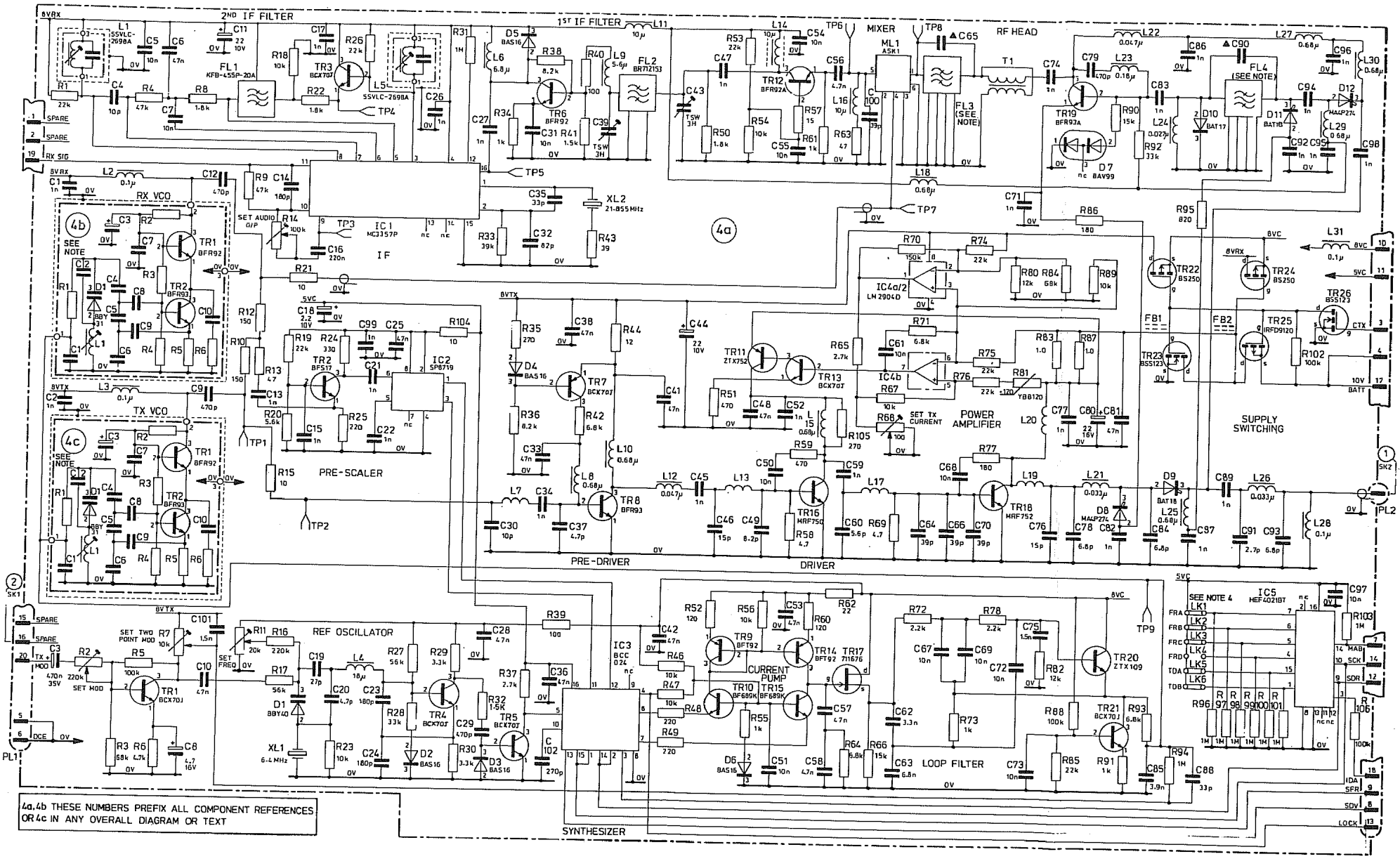
FRD(LK4)	FRC(LK3)	FRB(LK2)	FRA(LK1)	FL3 & FL4	Frequency (MHz)	REF
0	0	0	1		403 to 422.9875	A
0	0	1	0		407 to 426.9875	B
0	0	1	1		411 to 430.9875	C
0	1	0	0		415 to 434.9875	D
0	1	0	1		419 to 438.9875	E
0	1	1	0		423 to 442.9875	F
0	1	1	1		427 to 446.9875	G
1	0	0	0		431 to 450.9875	H
1	0	0	1		435 to 454.9875	J
1	0	1	0		439 to 458.9875	K
1	0	1	1		443 to 462.9875	L
1	1	0	0		447 to 466.9875	M
1	1	0	1		451 to 470.9875	N

Note: Other link combinations are not used by the PRM4515U.

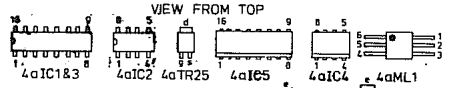
TABLE 3

Timeout Selection

TDB (LK6)	TDA (LK5)	Timeout (seconds)
0	0	30
0	1	60
1	0	90
1	1	120



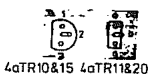
VIEW FROM TOP



4aD1 TO 12 INC
4bD1 & 4cD1
4bTR1 & 2
4cTR1 & 2

4aTR1,2,3,4,5,6, 7,8,9,12,13,14,19, 21,23 & 26

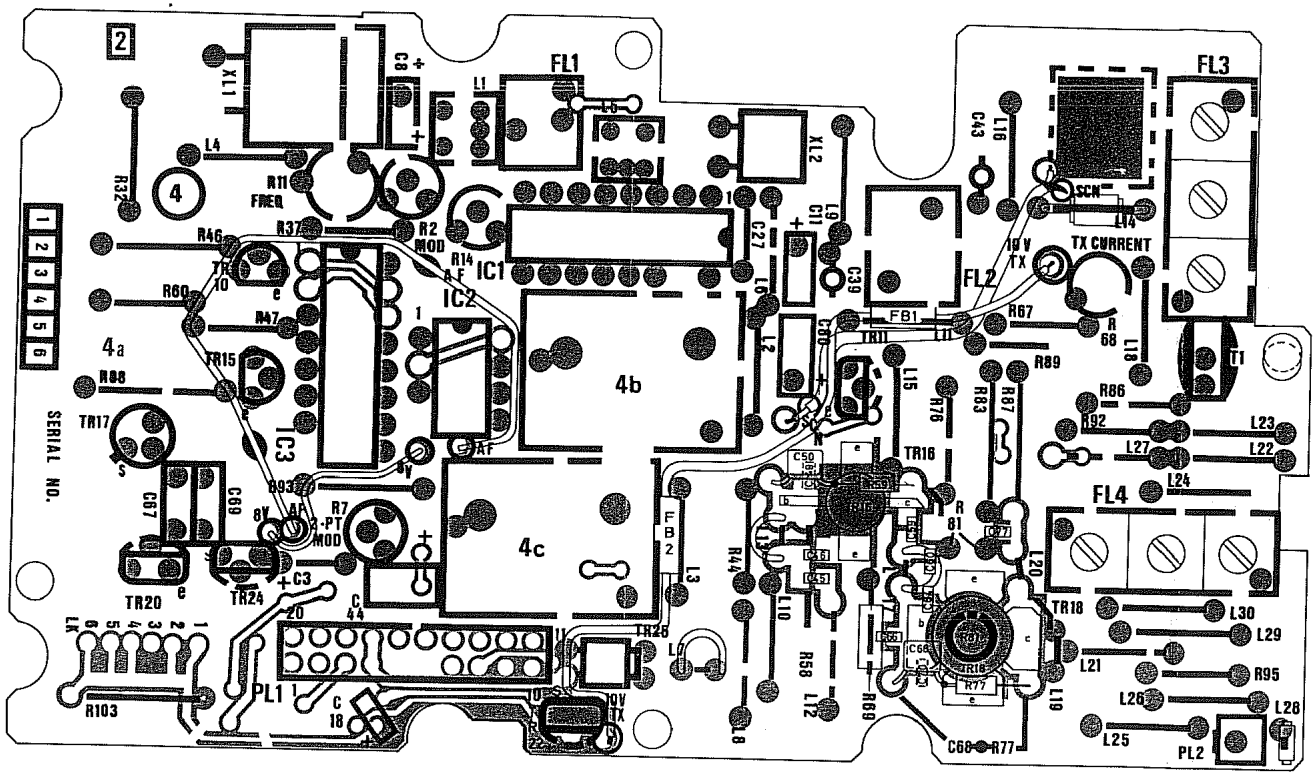
VIEW FROM BOTTOM



NOTES:-
1. UNITS 4b, 4c, AND FILTERS FL3, FL4 VARY DEPENDING ON FREQUENCY OF OPERATION. FOR PART Nos. SEE CHAPTER 9 OF THIS MANUAL.
2. ▲ DENOTES - COMPONENT, PART OF PCB (TRACK).
3. COMPONENTS NOT FITTED C40, R45, & R79.
4. LINKS L1 TO L6 AS SHOWN CONNECTED FOR 427-447MHz FREQUENCY OPERATION. CONNECTIONS FOR OTHER FREQUENCIES AND TIME OUTS SHOWN IN CHAPTER 4 TABLES 2 AND 3 OF THIS MANUAL.

RACAL
TH 7158 79280-141-10
F

Transceiver Board: Circuit Fig.4.15



RACAL
TH 7158 | 39280-650-10
E

Transceiver Board :
Top Track (Sheet 1)

Fig. 4.16

FUNCTIONAL TESTS AND ALIGNMENT

33 Functional tests and alignment procedures for the Transceiver Board are detailed in Tables 5 and 6. The tests check correct working of various parts of the circuit and can therefore be used to identify the source of a fault, and to confirm correct operation after a repair.

34 For the tests, operate the Transceiver Board with the remaining parts of a known-working PRM4515U and BCC test jigs TJ1117 and TJ1252 as shown in Fig 4.17. To allow access to all parts of the board, connect the Transceiver Board to the Control Board via Extender Cable TJ2013. Apply a 10 V (nominal) supply to the battery terminals of the PRM4515U, using Battery Adaptor TJ2017 (ensure correct polarity).

35 For the tests, program one channel for operation at F0 (lowest frequency used by the UUT) plus 10.0000 MHz. All tests are in Clear Mode, and the OFF/Volume switch can be at any position 1 to 6 unless otherwise specified in the procedures.

TYPICAL VOLTAGES AND WAVEFORMS

36 Typical voltages and waveforms are shown in Table 7. The board under test is set-up as for the functional tests (Para. 37), with access available to all parts and power connected. No other external inputs are used for the static tests.

37 Set the unit to Channel 0 and noise-on (OFF/Volume switch set to position 7).

EQUIPMENT REQUIRED FOR TRANSCEIVER BOARD TESTS

(1) DC Power Supply

Voltage	:	0 to 12 V
Current	:	1 A
Example	:	Farnell LT30-2

(2) RF Signal Generator

Frequency Range	:	500 MHz
Impedance	:	50 ohm
Output Level	:	-140 dBm to +13 dBm
Example	:	Hewlett Packard 8640B

(3) RF Power Meter

Frequency	:	500 MHz
Impedance	:	50 ohms
Power	:	3 Watts dissipation
Example	:	HP436A

(4) RF Spectrum Analyser and Tracking Generator

Impedance	:	50 ohms
Frequency Range	:	1-1200 MHz
Example	:	HP141T with HP8554B, HP8552B and HP8444A

(5) AF Function Generator

Frequency	:	10 Hz to 100 kHz
Level	:	0-3 V r.m.s.
Example	:	Philips PM5132

(6) Audio Analyser/Voltmeter

Frequency	:	10 Hz to 10 kHz
Example	:	HP339A

(7) Digital Multimeter (two required)

Voltage Range	:	0V to 10 V dc
Current Range	:	0 to 1 A
Example	:	Racal 4002

(8) Oscilloscope

Bandwidth	:	DC to 10 MHz
Impedance	:	1 mΩ
Example	:	Gould Advance OS3000A

plus a 10 M ohm probe

(9) Modulation Meter

Frequency	:	500 MHz
Deviation	:	Up to 10 kHz
Impedance	:	50 ohm
Filter	:	150 Hz notch
Example	:	Racal 9008 M

(10) RF Attenuator

Frequency	:	DC to 500 MHz
Impedance	:	50 ohms
Attenuation	:	Variable 0 to 110 dB, 3 W rating
Example	:	Telonic 8143A

(11) Frequency Counter

Frequency	:	500 MHz
Accuracy	:	Better than +/- 1 part in 10^7
Example	:	Racal 9917A Option 04A

(12) Test Aids

Extender Cable, 20-Way, TJ2013
Audio Interface Jig BCC TJ1117 (41117-100-10)
Battery Adaptor, TJ2017
Transceiver Board Alignment Jig BCC TJ1252 (41252-100-10)

TABLE 4

Interboard Connector Listing

Pin	I/O	Signal
PL1 (To/from Control Board)		
1		-
2		-
3	I	CTX. Transmit Control.
4	I	10 V Batt.
5		0 V.
6		0 V.
7	I	MAB. Crypto module absent.
8	I	SDV. Synthesiser variable divisor.
9	I	SFR. Synthesiser data frame.
10	I	8VB.*
11	I	5VB.*
12	I	SDR. Synthesiser reference divisor (and initialise register output enable).
13	0	OOL. Out of lock.
14	I	SCK. Synthesiser (and initialise register) clock.
15	I	SYN. Synthesiser power control.+
16	I	PA CON. Power amplifier control.+
17	I	10 V Batt.
18	0	IDA. Initialise data.
19	0	RX SIG. Received signal (demodulated).
20	I	TX MOD. Transmit signal (modulated).

* On the transceiver board, 8 VB ≡ 8 VC
5 VB ≡ 5 VC

\+ Not used in PRM4515U

TABLE 5

Transmitter Alignment

Use BCC test jigs TJ1252 and TJ1117.

Test No	Radio Mode & Frequency	Inputs/ Connections	Monitor	Limits and Adjustments
1	Clr, Tx F0+10.0000 MHz	Remove R15. Remove the two large screens.	RF output level using spectrum analyser connected to TP1 on TJ1252.	+0 dBm
2	As Test 1		RF output frequency. Measure with frequency counter connected to TP1 on TJ1252.	F0+10.0000 MHz ± 250 Hz Adjust R11
3	As Test 2	Connect a 50 ohm load (e.g. frequency counter) to TP1 on TJ1252.	DC voltage at TP9 (R93/R94) on the board using multimeter.	4.1-4.9 V
4	As Test 3	Connect RF signal generator output to TP2 on TJ1252 at F0+10.0000 MHz, +1 dBm. Set R68 fully clockwise. Connect ammeter in series with power to UUT with power supply output set to 10.0 V DC	(i) RF output on RF Power meter at PL2. (ii) DC current drawn. (iii) DC current drawn. (iv) RF output power	2 W 600-800 mA Adjust L17 and L19 for (i) and (ii) 600 mA Adjust R68 anti-clockwise 1.5 W Adjust L19

TABLE 5 (continued)

Test No	Radio Mode & Frequency	Inputs/ Connections	Monitor	Limits and Adjustments
5	As Test 4	Refit R15 and the two large screens. With the UUT isolated from TJ1252 test probes, apply 1 kHz square-wave, 1.3 V p-p at Pin A. TJ1117 set for WB	RF output, using modulation meter connected via attenuator. Use oscilloscope to monitor the demodulated output from the meter.	Optimum 1 kHz square wave Adjust R7
6	As Test 5	1 kHz sinewave 10 mV r.m.s. at Pin A. TJ1117 set to NB.	RF output, using modulation meter connected to PL2 via attenuator.	Deviation of 3.4 kHz (after the 150 Hz deviation has been subtracted) Adjust R2

TABLE 6

Receiver Alignment

Use BCC test jigs TJ1252 and TJ1117.

Test No	Radio Mode & Frequency	Inputs/ Connections	Monitor	Limits and Adjustments
1	Clr, Rx FO+10.0000 MHz	Remove ML1.	RF output level using spectrum analyser connected to TP7 on TJ1252.	> 0 dBm
2	As Test 1	Connect a 50 ohm load (e.g. spectrum analyser) to TP7 on TJ1252.	DC voltage at TP9 (R93/R94) on the board using multi-meter.	4.1-4.9 V
3	As Test 2	Connect tracking generator output to PL2 (antenna connection) via the attenuator. Level -30 dBm, Centre frequency : FO+10.00 MHz Scan width 5 MHz/div. Vert scale: 1 dB/div.	RF output level using spectrum analyser connected to TP8 on TJ1252.	Gain at FO+10.0000 MHz : > 7 dB Ripple over FO to FO + 20.000 MHz < 5 dB Adjust FL3 and FL4
4	As Test 3	Connect tracking generator output to TP6 via the attenuator at a level of -50 dBm, Centre frequency 21.400 MHz Scan width 5 kHz/div. Vertical scale: 1 dB/div.	21.4 MHz output level using using spectrum analyser connected to TP5 on TJ1252.	Ripple over 21.400000 MHz ±8 kHz: < 1.5 dB Output level >-50 dBm 3 dB band-width ± 10-12 kHz Adjust C39 and C43

TABLE 6 (continued)

Test No	Radio Mode & Frequency	Inputs/ Connections	Monitor	Limits and Adjustments
5	As Test 4	Connect RF signal generator to TP6 on TJ1252. Frequency 21.4000 MHz Level -100 dBm No modulation.	455 kHz output level using oscilloscope connected to TP4 on TJ1252.	Maximum peak to peak voltage Adjust L5
6	As Test 5	Connect RF signal generator to TP6 on TJ1252. Frequency 21.40000 MHz Level -100 dBm Modulation off.	DC voltage level at TP3 on TJ1252 (using multi-meter.	3.5 V dc Adjust L1
7	As Test 6	Refit ML1. Connect RF signal generator output to PL2 (antenna connection). Frequency: FO+10.0000 MHz Level: -100 dBm Deviation: 4 kHz Modulation frequency: 1 KHz	AC voltage at IC1/Pin 11 using oscilloscope.	1 kHz sine-wave 1.3 V p-p Adjust R14

TABLE 7

Reference Voltages

			RX, NOISE-ON			TX, AS RX UNLESS STATED		
			E (S)	B (G)	C (D)	E (S)	B (G)	C (D)
(Supply switching)	TR	22	8.0	9.7	0	8.0	0	8.0
		23	0	9.7	0	0	0	9.4
		24	8.0	0	7.9	8.0	9.4	0
		25	9.8	9.7	0	9.6	0	9.4
		26	0	0	9.7	0	5.0	0
(RECEIVER)	TR	3	7.2	7.9	7.9	0	0	0
		6	0.5	1.2	7.9	0	0	0
		12	1.6	2.3	7.8	0	0	0
		19	1.8	2.5	7.0	0	0	3.7
(Transmitter)	TR	7	0	0	0	7.6	7.0	2.6
		8	0	0	0	0	0.7	Approx 8.0
		11	0	0	0	9.1	8.5	7.5
		13	0	0	0	0.2	0.9	Approx 8.5
(SYNTHESISER)	TR	1	0	0	0	1.3	1.9	4.9
		4	2.4	3.0	5.3			
		5	0	0	6.4 MHz Sq Wave			
* VT varies from approx 3.5 to 5.5 Volts depending on Frequency of operation		9	8.0	7.9	7.9			
		14	8.0	7.9	VT*			
		10	5.2	1.1	7.9			
		15	5.2	1.1	VT*			
		17	VT±0.2	VT	7.9			
		20	VT-0.4 VT-0.8	VT±0.2	7.9			
		21	0.75	1.4	VT-0.4 VT-0.8			
		2	0.2	0.9	4.8			

IC	Pin	D.C. Volts		A.C. Volts		A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Clear N-On	Clear Tx	
1	1	7.8	0			
	2	7.1	0	Fig 1		
	3	7.8	0	Fig 2		
	4	7.8	0			
	5	1.0	0	Fig 3		
	6	1.0	0			
	7	1.0	0	Fig 4		
	8	7.8	0	Fig 5		
	9	3.7	0	Fig 6		
	10	1.9	0			
	11	2.0	0	Fig 7		
	12	0.8	0			
	13					
	14					
	15	0	0			
	16	2.0	0			

Pins 13 and 14 are not used

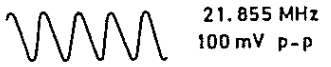


Fig 1

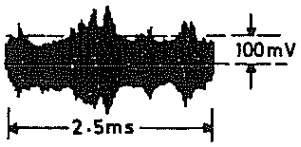


Fig 2

Fig 3

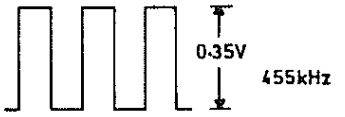


Fig 4

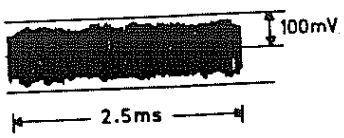


Fig 5

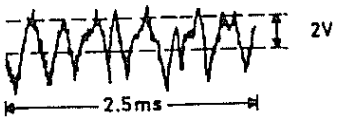


Fig 6

Fig 7

IC	Pin	D.C. Volts		A.C. Volts		A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Clear N-On	Clear Tx	
5	1	See Note				Pins 1, 4, 5, 6, 7, 15 are held L or H according to the preset options, as shown in Chapter 4, Tables 1 and 2
	2					
	3	H	H			
	4					
	5					
	6					Pins 2 and 12 are not used
	7					
	8					
	9	H	H			
	10	L	L			
	11	L	L			
	12					
	13	0	0			
	14	H	H			
	15					
	16	5.2	5.2			
3	1	0	0			
	2	0	0			
	3	5.2	5.2			
	4	0	0			
	5			Fig8	Fig8	
	6	5.2	5.2	Fig9	Fig9	
	7	5.2	5.2	Fig9	Fig9	
	8	0	0			

Fig 8

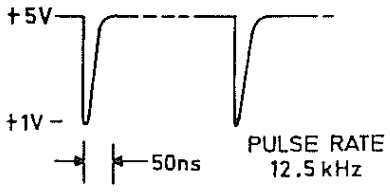


Fig 9

IC	Pin	D.C. Volts		A.C. Volts		A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Clear N-On	Clear Tx	
3	9					Pins 9 and 10 are not used
	10					
	11			Fig10	Fig10	
	12			Fig11	Fig11	
	13	0	0			
	14	0	0			
	15	0	0			
	16	5.0	5.0			
2	1			Fig12	Fig12	
	2	5.0				
	3			Fig10	Fig10	
	4	0	0			
	5	3.7	3.7			
	6	3.7	3.7			
	7	0	0			
	8	5.0	5.0			

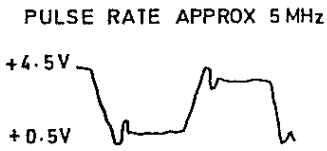


Fig 10

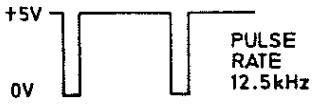


Fig 11

Fig 12

IC	Pin	D.C. Volts	
		Clear, Rx Noise ON	Clear Tx
4	1	0	6.4
	2	0	2.9
	3	0	2.9
	4	0	0
	5	0	2.9
	6	0	2.9
	7	0	0.8
	8	0	7.8

CHAPTER 5

CONTROL BOARD

CONTENTS

	Page
INTRODUCTION	5-1
BRIEF DESCRIPTION	5-1
Regulators and Reset	5-1
Control (Processor)	
Switch-on	5-2
Transmit	5-2
Receive	5-2
Standby	5-4
Frequency Control Data	5-5
Crypto Cipher Code Data	5-5
Control Data (From External Controller)	5-6
Warning Tone Generation	5-6
150 Hz Tone Squelch	5-7
Audio Amplifier and Volume Control	5-7
Transmit Modulation Buffer	5-8
DETAILED DESCRIPTION	5-8
Power, Switch-on, 8V Regulator	5-8
5V Regulator and Reset Generator	5-8
Low-Voltage Detector	5-9
External Supply and Protection	5-9
Processor (and I/O Interface)	5-10
EEPROM	5-11
Output Latches	5-11
CTS (and Other) Output Buffers	5-11
PTT/Data Detector and Driver	5-11
CRA and TON Buffers	5-15
Mode Switch Inputs	5-15
Channel Switch Inputs	5-15
Rx Signal and Warning Tone Routeing	5-16
Volume Switch Gates	5-16
Fixed Level Audio	5-16
Volume Control Circuit	5-17
Audio Power Amplifier	5-17
Squelch Detector (Part of)	5-18
Tx Signal Routing and Modulation Buffer Amplifier	5-18
FUNCTIONAL TESTS AND ALIGNMENT	
TYPICAL VOLTAGES AND WAVEFORMS	
EQUIPMENT REQUIRED FOR BOARD TESTS	

TABLES

Table No.

1	Direct Inputs to the Processor via the Data Ports
2	Direct Outputs from the Processor via the Data Ports
3	Latched Outputs from the Processor via ML11, ML12
4	Interboard Connector Listing
5	Functional Tests and Alignment
6	Static Reference Voltages

ILLUSTRATIONS

Fig. No.

5.1	Power Regulation and Switching
5.2	Control Board : Block Diagram
5.3	Processor : Control Inputs and Outputs
5.4	150 Hz Squelch Tone Route
5.5	Audio Amplifier and Volume Control
5.6	8V and 5V Regulators
5.7	Low-Voltage, Fail, and Protection
5.8	Processor
5.9	Volume Control
5.10	Audio Power Amplifier
5.11	Squelch Tone Filter and Slicer
5.12	Transmit Modulation Buffer Amp
5.13	Frequency Word and Cipher Code Header : Formats
5.14	Control Data (From External Controller) : Formats
5.15	Control Board : Circuit
5.16	Control Board : Layout
5.17	Synthesiser Data : Timing Diagram
5.18	Start of Fill Data : Timing Diagram
5.19	End of Fill Data : Timing Diagram

CHAPTER 5

CONTROL BOARD

INTRODUCTION

1 The Control Board contains the voltage regulators, with supply switching, protection and control reset facilities; the microprocessor that controls the unit's operations; squelch system; audio output amplifier and volume control circuit; transmit modulation buffer amplifier; and switch decoding circuit.

BRIEF DESCRIPTION (Fig. 5.2, 5.15)

Regulators and Reset (Fig. 5.1)

2 When the unit is switched-on, the 8V regulator powers the 8V rail from the 10V battery supply, and the 5V regulator automatically powers the 5V rail when the 8V rail is established. The PIN C line is bidirectional: it can be used to power external equipment or an external dc supply can power the radio.

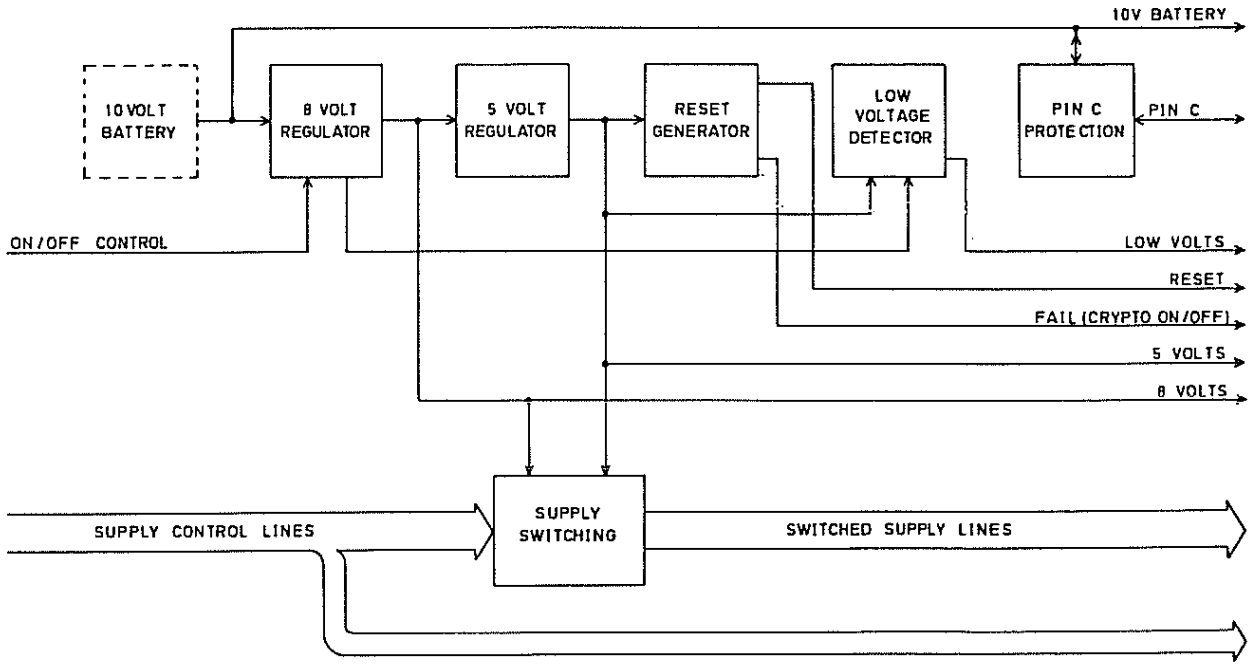


Fig 5.1 Power Regulation and Switching

3 The power-up reset generator resets the processor to its initial state and, if the unit is set for secure operation, a slightly delayed version of the reset signal switches on the crypto. The low-voltage detector informs the processor when battery power starts to go low.

4 To reduce current consumption, the processor switches-off various circuits when they are not in use. It switches some supplies on the Control Board, and it switches others by sending control signals to the applicable circuits on other boards.

Control (Processor) (Fig. 5.3)

5 The microprocessor controls the unit according to the requirements of the Mode, Channel and OFF/Volume switches, preset initial settings from links in the unit, PTT, WIB, FLA signals, and any pwm (pulse width modulated) data inputs via the PTT line. When the OFF/Volume switch is moved from the OFF position and switches-on the power rails, it resets the processor to the start of its program.

Switch-on

6 The processor sets up its output ports, reads the initialise register to determine the unit's operating frequency range, transmit timeout and whether a crypto is fitted, and loads its internal RAM with frequency information (divisors) from the EEPROM. It energises the applicable parts of the unit for transmit operation, if PTT is active; for receive operation, if 150 Hz tone squelch or digital squelch is present (or squelch-open is selected); and produces any necessary warning tones. If none of these actions is required, the processor puts the unit into standby mode (Para. 10).

Transmit

7 A low signal of more than 1 ms duration on the PTT line interrupts the processor and initiates a transmit operation. The transmit operation continues until both PTT and TON (from the crypto) are no longer active (TON allows for the additional time required by the crypto circuits), provided the time-out period has not expired. The processor sets its control outputs for the applicable transmit operation (secure, clear, wideband), loads the transmit frequency divisor into the synthesiser, enables the transmit circuits, illuminates the Transmit indicator (TX LED) and starts its internal time-out timer. For clear transmission it also generates a 150 Hz squelch tone to add to the transmitter signal, and a slow-pip warning which goes via the receive audio circuits to the audio output. For secure transmission it also powers-up the crypto circuit then sets it to transmit (after a delay of about 3.3 ms). After the transmit operation, the processor reloads the synthesiser with the divisor used for receive operations (on that channel).

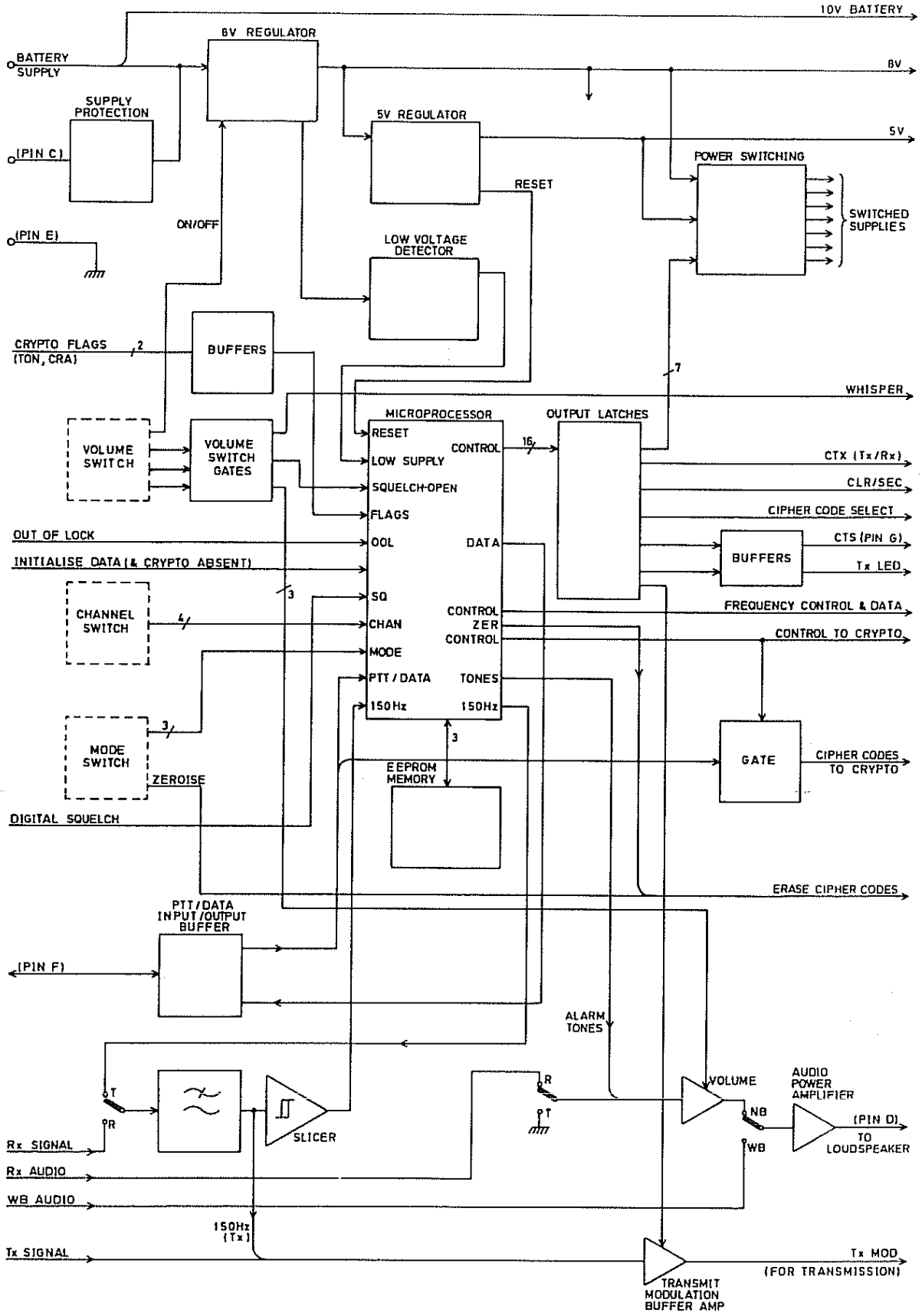


Fig 5.2 Control Board: Block Diagram

Receive

8 On receipt of a 150 Hz squelch tone, the processor enables the receive audio circuits. If squelch-open is selected (by the OFF/Volume switch) the circuits are continuously enabled.

9 On receipt of a 16k bit/sec digital squelch the processor responds as follows:

(1) If the unit is configured for secure operation (ie. secure mode is selected, wideband is not, and a crypto is fitted), the processor enables the receive audio circuits and the crypto. The unit outputs the decrypted message (provided it has the correct cipher code).

(2) If clear mode is selected, and there is a crypto fitted, the encrypted message goes via the clear route and emerges as 'white' noise.

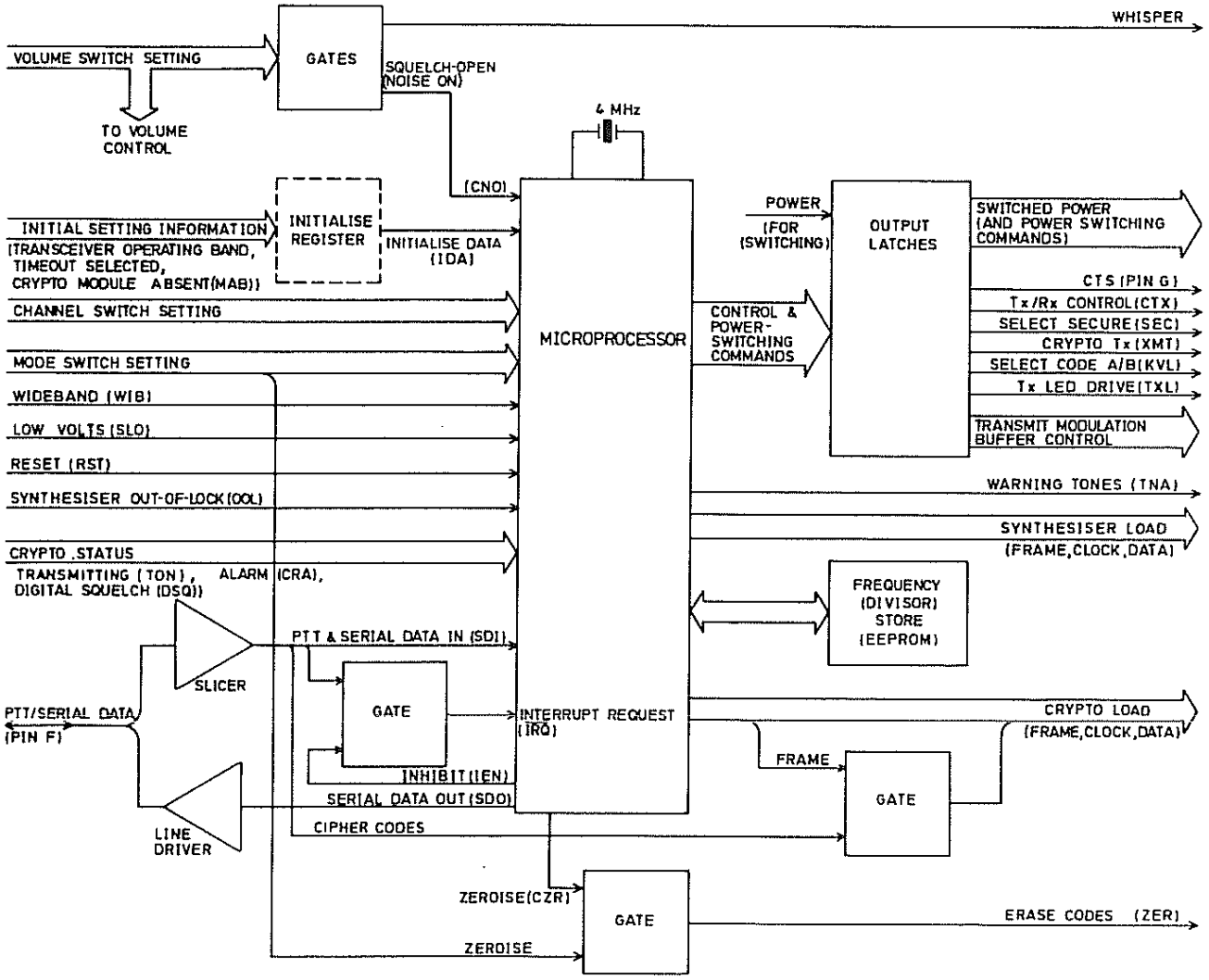


Fig 5.3 Processor: Control Inputs and Outputs

(3) If clear mode is selected, but there is no crypto fitted, the processor ignores the squelch.

(4) If wideband is selected, the squelch is ignored.

Standby

10 When the unit is switched-on but is not transmitting, receiving, or sending warning tones, the processor removes power from the circuits that are not in use. The receiver circuit must remain on in case a squelch signal arrives, the 16k bit/sec signal detector remains on to detect a digital squelch, and the synthesiser is on so that the arrival of a 150 Hz tone squelch can be detected. When in standby mode, the processor checks the output from the low-voltage detector and, if the battery state is low, routes bursts of receiver noise to the audio output for 20 ms every 200 ms. (If squelch-open is selected, the unit is in receive mode (ie. not in standby mode)).

Frequency Control Data

11 The transmit and receive frequencies to be generated by the synthesiser enter as 4k bit/sec pwm data on the PTT line. The arrival of data interrupts the processor, which interprets the header at the start of the 52 bit word. The data format is shown in Fig. 5.13. The header includes the channel number (bits 13 to 16) and indicates whether the frequency information is for transmit or receive (bit 9). The processor calculates the divisor that it will have to load into the synthesiser to achieve the required frequency, and stores this information, against the channel number, in the EEPROM. It echoes the serial data word back to its source via the PTT line, with bit 7 set to 0 instead of 1, to acknowledge that it has been accepted. If an out-of-range frequency arrives, the processor rejects it and sends no acknowledgement.

12 To load the synthesiser the processor outputs a Frame signal which enables the synthesiser to accept new data, and clocks the variable divisor, for dividing the VCO feedback, and the reference divisor, for dividing the reference clock, to the synthesiser. The divisors go as two data streams (SDV, in which the last 11 bits are valid, and SDR, in which the last 21 bits are valid), with common frame (SFR) and clock (SCK) signals.

Crypto Cipher Code Data

13 Data for the crypto enters as pwm data on the PTT line, and interrupts the processor, which interprets the header. The data format is shown in Fig. 5.13. The processor produces a frame signal (FFR). This gates the incoming cipher code data directly through to the crypto, and enables the crypto to accept the data, which is clocked-in by SCK (the same line as the processor uses to clock frequency data to the synthesiser).

Control Data (From External Controller)

14 Data from an external controller, which overrides the unit's own controls, enters as pwm data on the PTT line. It interrupts the processor, which interprets the header, decodes the word, resets its control outputs to carry-out the requested action, and echoes the word with bit 7 set high as an acknowledgement. The word may be a 32-bit channel request word, with the number of the new channel; a 52-bit mode word to change clear/secure, or squelch open/closed; a 52-bit control word to change secure A/B; or a 32-bit zeroise command to erase the stored cipher codes. The data formats are shown in Fig. 5.14. If the processor receives a secure mode word and control word but has no crypto fitted, it replies with a clear mode word (and ignores the command).

Warning Tone Generation

15 The processor produces warning tones (TNA) which it routes to the audio output. It can also produce a chuff-chuff warning by switching bursts of noise through. If squelch-open has been selected, the processor overrides this command so that the warning is audible. Because the tones can be produced only one at a time, the priority is as follows:

(1) Error tone.
(2) Crypto Alarm.
(3) Rapid pips (transmit mode only).
(4) Slow pips.
(5) Battery low (standby mode only).

16 The error tone is two-tone continuous alarm, 1 kHz for 520 ms alternating with 2 kHz for 520 ms. It occurs when:

(1) The synthesiser is out of lock (OOL signal from synthesiser).
(2) The secure mode is selected but the crypto module is not fitted (MAB, Module Absent signal detected via initialise register).
(3) The transmit time has been exceeded (the time is set by TDA and TDB via the initialise register).
(4) Transmit has been inhibited owing to crypto alarm (CRA).

17 The crypto alarm is a continuous 1 kHz tone produced when the crypto does not have a valid cipher code (it sends a CRA (Crypto Alarm) signal to the processor).

18 Rapid pips, 66 ms bursts of 2 kHz tone repeated every 230 ms indicate that only 5 seconds of transmission time remains.

19 Slow pips, 33 ms bursts of 2 kHz tone repeated every 2 seconds indicate that the message being transmitted or received is in clear mode. Therefore, when transmitting, it indicates that the unit is set for clear transmission. When receiving it indicates that the message is being received in clear mode (ie. 150 Hz tone is present) regardless of the unit's clear/secure setting. Slow pips are also generated when the unit is set for squelch-open.

20 For the battery-low warning (when the unit is in standby mode, ie. not transmitting or receiving) the processor opens and closes the receiver squelch to provide a chuff-chuff noise, with 20 ms bursts every 200 ms. Also, when in the transmit mode it flashes the transmit indicator half a second on, half a second off, to indicate a low battery.

150 Hz Tone Squelch (Fig. 5.4)

21 The 150 Hz tone squelch system is software-based. In transmit mode the processor produces the tone and switches it, after filtering, onto the transmit signal route to the transmit modulation buffer. In receive mode, the incoming signal is low-pass filtered to remove the audio, then a slicer converts it to a squarewave suitable for use by the processor in its detection operation. This is inhibited while the processor is starting-up, and during interrupts.

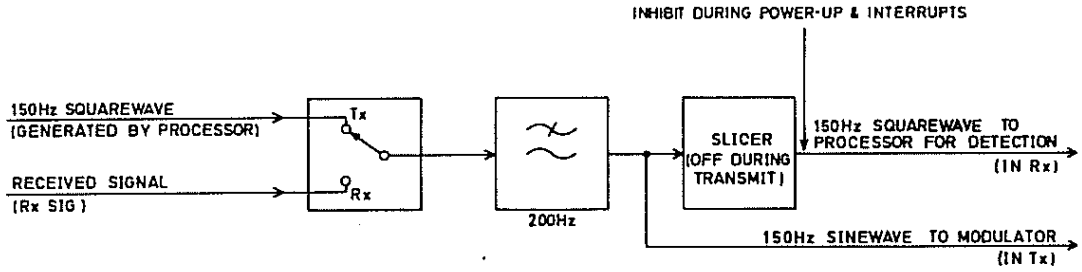


Fig 5.4 150 Hz Squelch Tone Route

Audio Amplifier and Volume Control (Fig. 5.5)

22 The Rx Audio signal (ie. RX SIG after processing (as necessary) and filtering on the Crypto Board) is combined with a warning tone (if applicable) and the result goes via one of eight resistors, decided by the position of the OFF/Volume switch. The chosen resistor is the input resistor to the audio amplifier and therefore affects the gain of the output.

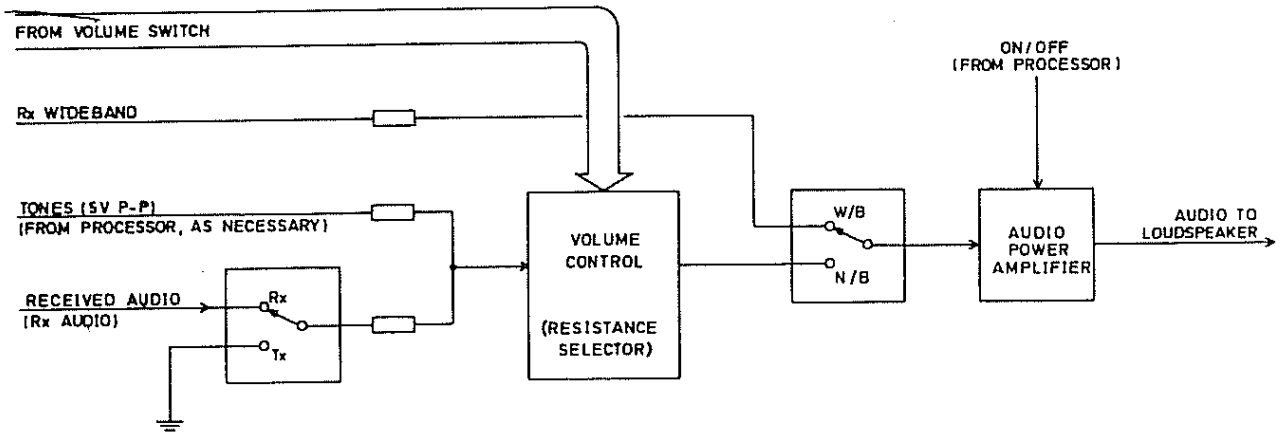


Fig 5.5 Audio Amplifier and Volume Control

Transmit Modulation Buffer

23 The transmit modulation buffer allows the processor to control the level of the TX MOD signal such that it can be transmitted by a VHF low-band, VHF high-band or UHF Transceiver Board. The processor can select one of four amplifier gains according to the transmit frequency that is in use. One gain is used in UHF (ie. by the PRM4515U).

DETAILED DESCRIPTION (Fig. 5.15)

Power, Switch-on, 8V Regulator (Fig. 5.6)

24 The 8V regulator produces the 8VB supply from the 10V BATT input (ZP1) when the VOL D line (SK5/2) from the OFF/Volume switch is high. VOL D high switches-on FET TR3, which switches-on FET TR2, thus establishing the 8VB rail.

25 Transistor TR4 controls the regulation. Its base is fed with divided feedback from the 8VB rail via potentiometer R6, and it drives transistor TR1 which, in turn, controls the FET's gate voltage and hence the rail voltage. Zener diode D1 provides the reference voltage for TR4, and the potentiometer adjusts the feedback to TR4 and thus sets the 8VB rail voltage.

5V Regulator and Reset Generator (Fig. 5.6)

26 When the 8VB rail is established, the voltage to the inverting input (pin 2) of op amp ML1 causes a low output (pin 6), which turns-on FET TR5. The op amp controls the regulation. Its non-inverting input (pin 3) receives divided feedback from the 5VB rail via R11, R12, R13, which it compares with a fixed reference at its inverting input. The fixed reference is derived from the 8VB rail via R8, R98, by zener diode D2. Potentiometer R13 adjusts the feedback to the op amp and thus sets the 5VB rail voltage.

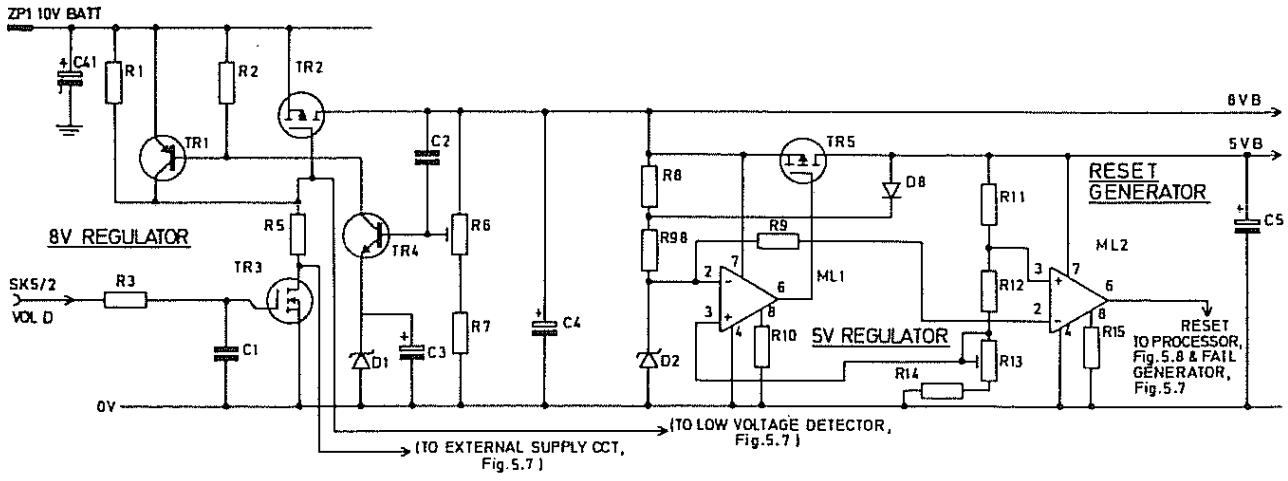


Fig 5.6 8 V and 5 V Regulators

27 Op amp ML2 compares the divided 5VB input to pin 3 with the reference provided by D2 via R9 to pin 2, and, when the rail voltage reaches 90% (ie. 4.5V), the op amp produces a high output (pin 6). This high-going edge goes to the processor (ML7, pin 1), which resets to its initial conditions then starts to operate. The Reset signal also goes to the fail generator.

28 On receipt of the high Reset signal, schmitt NAND gate ML5C produces a low output (pin 10), after a slight delay caused by R24/C7. While the gate's output is low it gates the SEC signal through NOR gate ML6b (inverted), as Fail (SK2/4) to switch the crypto on/off.

Low-Voltage Detector (Fig. 5.7)

29 When the 10V BATT line starts to fall, the gate voltage of FET TR2 (in the 8V regulator circuit) drops, so the FET turns-on more to compensate for the battery voltage drop. When the voltage at the FET's gate has fallen sufficiently for FET TR6 to turn-on, TR6 outputs a PA CON signal, and when the voltage to pin 2 of op amp ML3 exceeds the reference input to pin 3 (divided-down from 5VB), the op amp's output goes low. This goes to the processor as SLO (ML7, pin 28); if transmitting, the processor flashes the Transmit indicator (TX LED); if standing-by the processor causes short pulses of noise on the audio output.

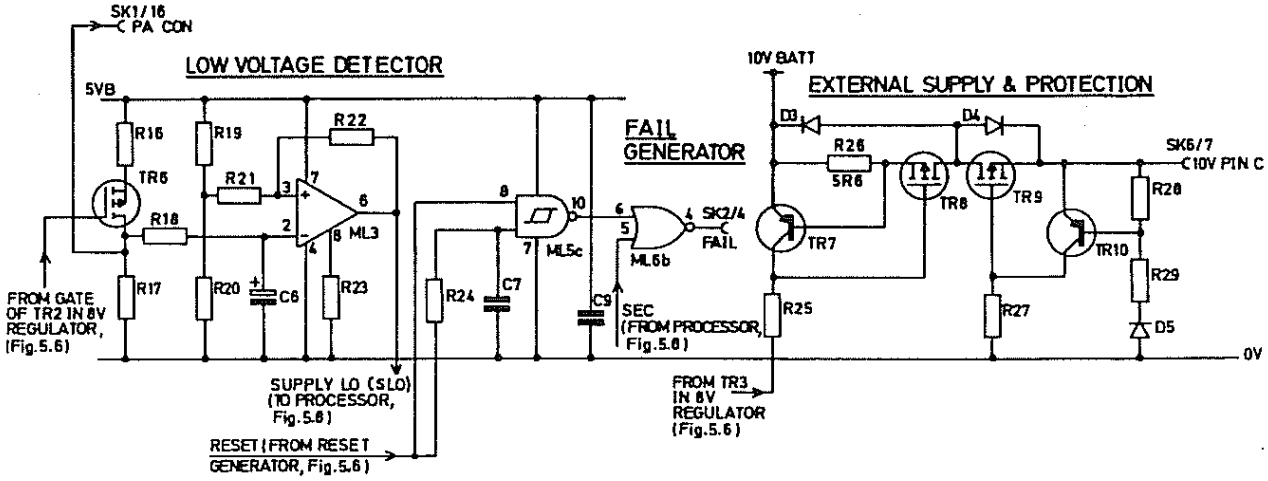


Fig 5.7 Low-Voltage, Fail and Protection

External Supply and Protection (Fig. 5.7)

30 After switch-on, FET TR3 in the 8V regulator circuit is on, and this switches-on FET TR8, thus connecting the 10V BATT supply through to 10V PIN C (SK6/7) for use by external equipment. The output is limited to a nominal 100 mA. Transistor TR7 senses the voltage across R26 and if too much current is drawn the transistor switches on, thus turning-off TR8.

31 If an external supply is connected to 10V PIN C (SK6/7) to power the radio, it must be between battery voltage and 15.6V. If a higher voltage is applied, diode D5 conducts. This switches-on transistor TR10 and switches-off FET TR9 until the over-voltage condition is removed.

Processor (and I/O Interface) (Fig. 5.8)

32 The processor, ML7, is an MC146805G2 8 bit register-oriented microcomputer, with 112 bytes of RAM (random access memory) and 2096 bytes of EPROM (read-only memory) built-in, and 32 bidirectional I/O (input/output) lines via four ports A, B, C, D. A clock generator, ceramic resonator CR1 plus associated components, provides a 4MHz clock signal which times the processor's operations.

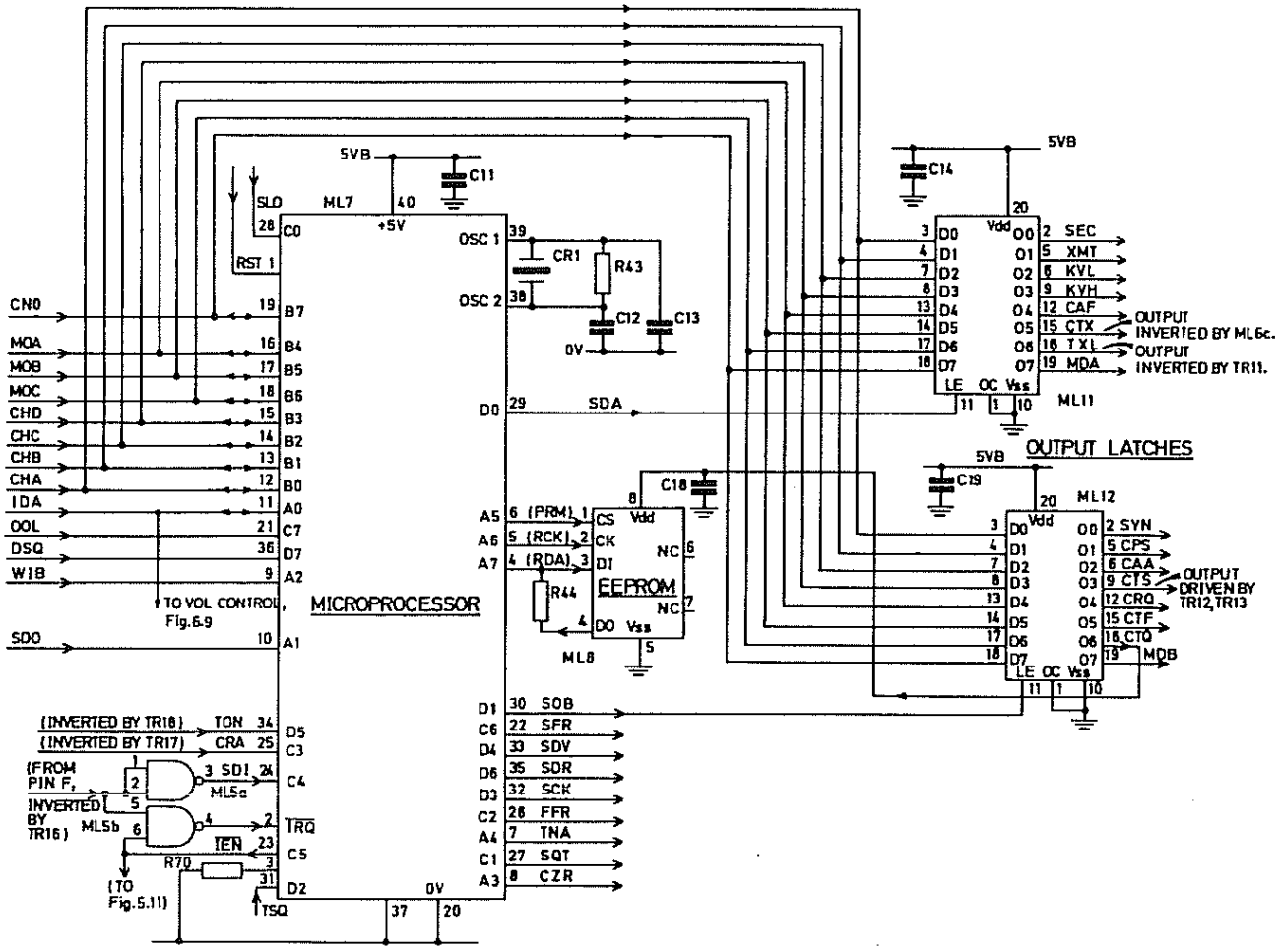


Fig 5.8 The Processor

33 Basically, when activated by the Reset signal, the processor starts to work through the program stored in its (pre-programmed) ROM. It carries-out the program instructions, which include reading the various control and status signals that it receives via its I/O ports. According to the requirements of these inputs, it goes to a particular part of its program, which enables it to produce a set of control outputs, via the I/O ports, that set the unit to the required operating state.

34 The $\overline{IRQ}$ (Interrupt Request) input (pin 2) allows an external device to interrupt the processor so that it jumps to another part of its program and carries-out the requirements of the interrupting device, changing its I/O lines as necessary. The direct inputs to the processor are shown in Table 1, direct outputs are in Table 2, and outputs latched by the SOA and SOB outputs are in Table 3.

EEPROM (Fig. 5.8)

35 The EEPROM, ML8, a 1024-bit electronically-erasable programmable memory, stores frequency information. It is powered when CTQ from the processor (ML12, pin 16) is high to pin 8. CS (pin 1) high selects the device. Pulses to CK (pin 2) clock data in via DI (pin 3) and out via DO (pin 4).

Output Latches (Fig. 5.8)

36 The output latches, ML11, ML12 are tri-state D-type flip-flops. LE (pin 11) high latches the D inputs through to the corresponding outputs, where they remain until the next high-going edge of LE. LE for ML11 is SOA from the processor (pin 29) and for ML12 it is SOB (pin 30). The outputs are shown in Table 3.

CTS (and Other) Output Buffers

37 The CTS output from the output latches is buffered by FETs TR12 and TR13. When CTS is low, TR12 switches-on and TR13 switches-off, thus making the PIN G output (SK6/5) low (pulled-down via external 4k7 resistors). TXL is buffered by transistor TR11. When TXL is low, the transistor is on and TXL (SK7/1) is high to illuminate the transmit indicator (TX LED). CTX is inverted by NOR gate ML6c, so CTX from SK2/13 is low for transmit.

PTT/Data Detector and Driver

38 PTT (SK6/2) low switches-on transistor TR16. Schmitt NAND gate ML5b inverts the transistor's output so $\overline{IRQ}$ (Interrupt Request) to the processor (ML7, pin 2) goes low. SDI (Serial Data Input) to the processor (pin 24) via ML5a also goes low. The processor makes IEN (Interrupt Enable, pin 23) low to disable further interrupts via ML5b until it has processed the current interrupt. It continues to receive the SDI signal. This may be a continuous signal, in which case the processor recognises PTT and goes into its transmit

routine. Alternatively, it may be pulse-width modulated data from an external device, in which case the processor interprets the header and carries out the required operation, and sends a reply on its SDO (Serial Data Out) line (pin 10). High outputs on SDO switch-on transistor TR15, which drives the PTT line (SK6/2) low, so the reply goes via the PTT line inverted. When the processor's FFR (Frame) output (pin 26) is high, data received via TR16 goes via AND gate ML4a as FDA (SK2/29). (This is cipher codes for the crypto).

TABLE 1

Direct Inputs to the Processor via the Data Ports

Signal Name	Port	Active	Description
CHA	B0	H	Binary coded inputs from channel switch. (CHA is the lsb, CHD the msb).
CHB	B1	H	
CHC	B2	H	
CHD	B3	H	
CNO	B7	H	Squelch override input from OFF/Volume switch (Squelch-open (noise-on)).
CRA	C3	H	Alarm tone select from Crypto.
DSQ	D7	H	Digital squelch.
IDA	A0	H	Serial data from initialise register (on Transceiver Board).
MOA	B4	H	Mode select bits (MOC is not used). (MOA is the lsb, MOC the msb). 00 = SEC B; 10 = CLR; 01 = SEC A; 11 = ZEROISE.
MOB	B5	H	
MOC	B6	H	
OOL	C7	H	Synthesiser out of lock.
RDA	A7	H	EEPROM serial data (frequency information).
SDI	C4	L	Serial data and PTT input.
SLO	C0	L	Supply voltage low indicator.
TON	D5	H	Crypto transmitting.
TSQ	D2	H	Tone input for squelch detection.
WIB	A2	H	Wideband select (forces clear mode, and inhibits economise).

TABLE 2

Direct Outputs from the Processor via the Data Ports

Signal Name	Port	Active	Description
CZR	A3	H	Zeroise crypto cipher codes.
FFR	C2	H	Crypto fill Frame signal.
TAC	A0	H	Tone Amplitude Control. Increase volume for alarm-tone short pips.
IEN	C5	H	Interrupt enable.
PRM	A5	H	EEPROM chip select.
RCK	A6	H	EEPROM clock.
RDA	A7	H	EEPROM serial data (frequency information).
SCK	D3	H	Clock for synthesiser load, crypto fill, and reading the initialise register.
SDO	A1	H	PWM serial data output (inverted version output to pin F).
SDR	D6	H	Synthesiser reference divisor data, and initialise register data output enable.
SDV	D4	H	Synthesiser variable divisor data.
SFR	C6	H	Synthesiser data Frame signal.
SOA	D0	H	Enable output latches ML11.
SOB	D1	H	Enable output latches ML12.
SQT	C1	H	150Hz squelch tone signal output.
TNA	A4	H	Warning tones.

See also Table 3 for the latched outputs.

TABLE 3

Latched Outputs from the Processor via ML11, ML12

Signal Name	Latch/ Pin	CPU Port	Active	Description
CAA	12/6	B2	H	Audio amplifier power supply control.
CAF	11/12	B4	L	Audio filter power supply control.
CPS	12/5	B1	H	Crypto clock generator power supply control. Permanently high.
CRQ	12/12	B4	H	Tone squelch filter and slicer power supply control.
CTF	12/15	B5	H	Transversal filter power supply control.
CTQ	12/16	B6	H	EEPROM power supply control.
CTS	12/9	B3	L	Clear to send, any squelch or any warning tone (to pin G).
CTX	11/15	B5	L	Transmit control.
KVL	11/6	B2	H	Crypto cipher code select. (KVH is not used). KVL = 0 for SEC A, 1 for SEC B). (KVL is held low during fill operation).
KVH	11/9	B3	H	
MDA	11/9	B7	H	Control transmit modulation buffer amp (and hence level of TX MOD).
MDB	12/9	B7	H	
SEC	11/2	B0	L	Secure select; Crypto enable.
TXL	11/16	B6	L	Transmit indicator (TX LED) control.
XMT	11/5	B1	H	Crypto transmit control.

CRA and TON Buffers

39 The CRA and TON signals are from the power backed-up Crypto Board, so transistors TR17, TR18 provide isolation for these two lines when the Control Board is not powered-up.

Mode Switch Inputs

40 The MOC, B, A inputs (SK3/5, 4, 1) from the Mode switch go straight to the processor. The inputs are binary coded, as shown in Table 1. MOD (SK3/2), Zeroise, low to erase the stored cipher codes, leaves the board as ZER (SK2/9). CZR high from the processor (ML7, pin 8) also makes ZER low: it switches-on transistor TR14.

Channel Switch Inputs

41 The CHD, C, B, A inputs (SK4/3, 6, 5, 2) from the Channel switch go straight to the processor. The inputs are in BCD form, as shown in Table 1.

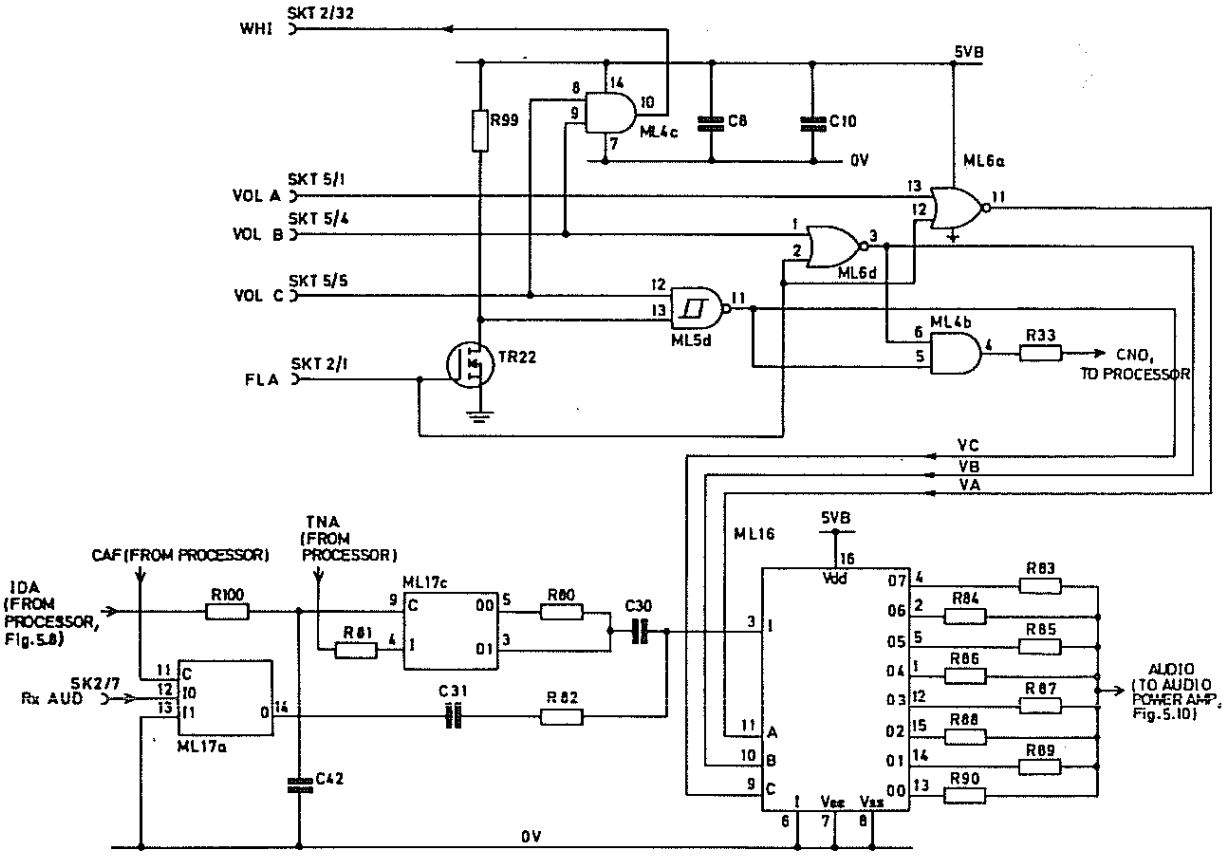


Fig 5.9 Volume Control

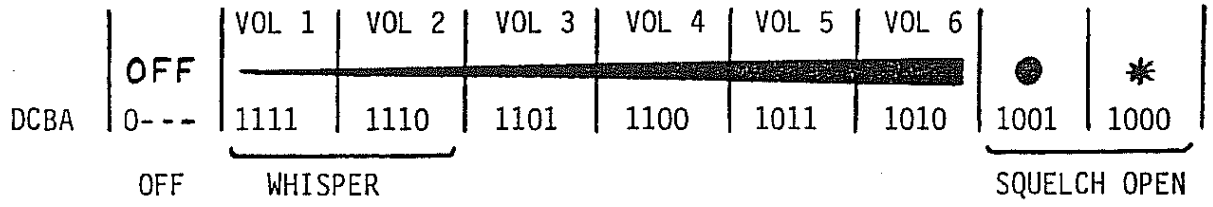
Rx Signal and Warning Tone Routeing (Fig. 5.9)

42 The received signal RX SIG (from the Transceiver Board) enters the Control Board via SK1/19 and goes to the squelch detect circuits (Para. 49). It also leaves the board via SK2/3 for processing on the Crypto Board, and returns as RX AUD (SK2/7). The processor switches it through analogue switch ML17a (pin 12 to pin 14), with CAF (ML11, pin 15) low, to the volume control circuit. Any necessary warning tones, TNA (ML7, pin 7), go via switch ML17c onto the audio line to the volume control. The level of the warning tones in relation to the received audio is determined by resistors R80, R81, R82. Two alarm levels are available: for the higher level, IDA high from the processor (ML7, pin 11) to pin 9 of switch ML17c, switches the warning tones through R81; for the lower level, IDA low switches the tones through R80. The higher level is used for short pips so that they have a similar 'apparent' volume to the continuous warning tone.

Volume Switch Gates (Fig. 5.9)

43 The VOL C, B, A (SK5/5, 4, 1) BCD signals from the OFF/Volume switch go to the volume switch gates; VOL C switches the power on/off (Para. 24). The three volume control signals, VOL C, B, A, inverted by NAND gate ML5d and NOR gates ML6d, ML6a become VC, VB, VA control signals for the volume control circuit (Para. 46). VC, VB, VA represent a binary number (VA is lsb), with 0 for the lowest volume.

44 For the lowest two volumes, VOL C and VOL B are both high so AND gate ML4c produces a high WHI (Whisper) output (SK2/32). This goes to the Crypto Board where it increases the Mic sensitivity. For the highest two volumes, VOL C and VOL B are both low. The outputs from NAND gate ML5d and NOR gate ML6d are both high, so AND gate ML4b produces a high output. This goes to the processor (ML7, pin 19) as CNO to select squelch-open (noise-on).



Fixed Level Audio (Fig. 5.9)

45 When FLA (SK2/1) is high (i.e. 1mA has been detected on the Mic input by the Crypto Board) it forces the VB and VA outputs from NOR gates ML6d and ML6a low, and, after inversion by FET TR22, forces the VC output from NAND gate ML5d high. It thus overrides the OFF/Volume switch and sets the VC, VB, VA outputs to select VOL 5.

Volume Control Circuit (Fig. 5.9)

46 Multiplexer ML16 receives the audio signal at pin 3, and switches it out via one of its O0 to O7 outputs, as selected by the binary number 0 to 7 on the VC, VB, VA lines to its CBA inputs (pins 9, 10, 11). Each route goes via a resistor: for minimum volume the O0 output goes via the highest value resistor, R90; for the highest volume, the O5 output goes via R85. The resistors R90, R89, R88, R87, R86, R85 provide 6 dB steps in volume. R84 is for medium volume (VOL 3) with squelch-open, and R83 is for high volume (VOL 6) with squelch-open. The resistors form part of the gain control of the audio power amp.

Audio Power Amplifier (Fig. 5.10)

47 The output from the volume control circuit goes to switch ML17b (pin 2). WIB low (from the processor, ML7, pin 9) to pin 10 switches the audio signal through (via pin 15) to the audio power amplifier. When WIB is high, the received wideband signal (WB Audio, SK2/31) is switched through instead.

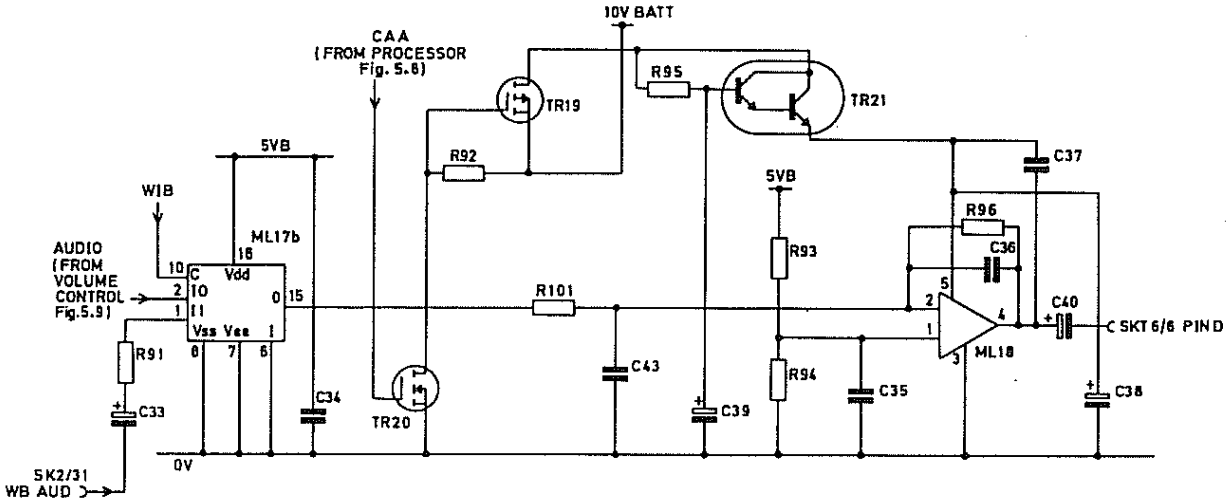


Fig 5.10 Audio Power Amplifier

48 The audio power amplifier, op amp ML18 plus associated components, amplifies the audio signal to loudspeaker levels (SK6/6). The gain is set by R96 plus one of R83 to R90, or, for wideband operation, R91. The processor makes CAA (ML12, pin 6) high to switch power to the amplifier. CAA high switches-off FET TR2, so the 10V BATT supply powers the amp via FET TR19 and darlington transistors TR21. Resistor R95 and capacitor C39 ensure a smooth start-up.

Squelch Detector (Part of) (Fig. 5.11)

49 When CTX from the processor (ML11, pin 15) is high (ie. the unit is not transmitting), switch ML9c switches through RX SIG (pin 3 to pin 4). The 200 Hz low-pass filter, op amp ML14 plus associated components, removes the high frequencies from the signal, and the slicer, op amp ML15 (powered by CTX) converts it to 5V peak-to-peak form. The processor receives the output from the op amp (pin 1) as TSQ (ML7, pin 31), and detects the 150 Hz squelch tone.

50 The TSQ input is held low until Reset has gone high and $\overline{\text{TEN}}$ is high. When either of these signals is low (i.e. at power-up and during an interrupt), the low output from AND gate ML4d inhibits the detection of tone squelch.

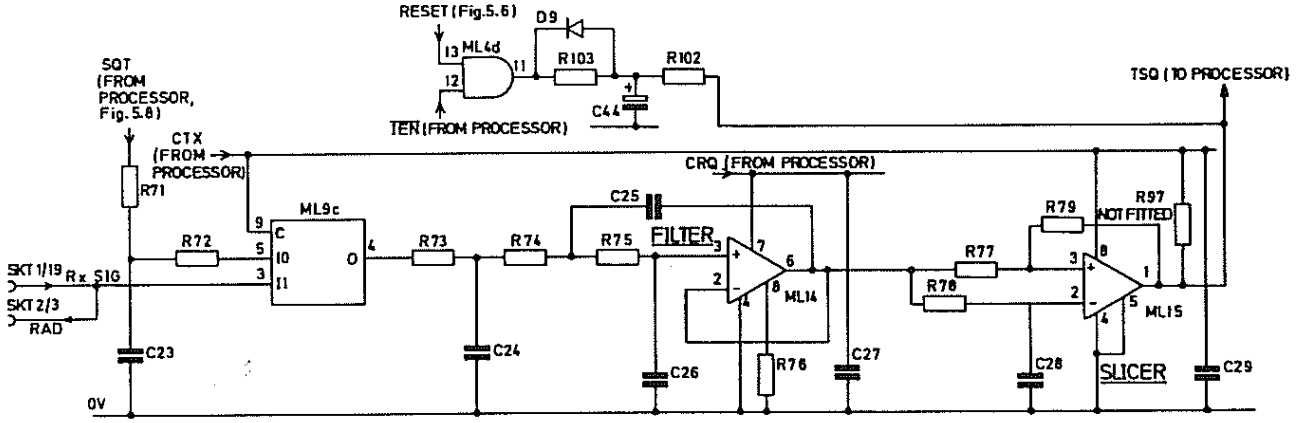


Fig 5.11 Squelch Tone Filter and Slicer

51 When CTX is low (ie. the unit is transmitting), switch ML9c switches through SQT, the 150 Hz squelch tone signal (pin 10 to pin 4) from the processor (ML7, pin 27). This goes via the 150 Hz filter and R53 and joins the Tx SIGNAL route to the transmit modulation buffer amplifier.

Tx Signal Routeing and Modulation Buffer Amplifier (Fig. 5.12)

52 The transmit modulation buffer amplifier, op amp ML10 plus associated components, adjusts the modulation level of TX SIGNAL (SK2/28) to suit the TX VCO circuits (on the Transceiver Board).

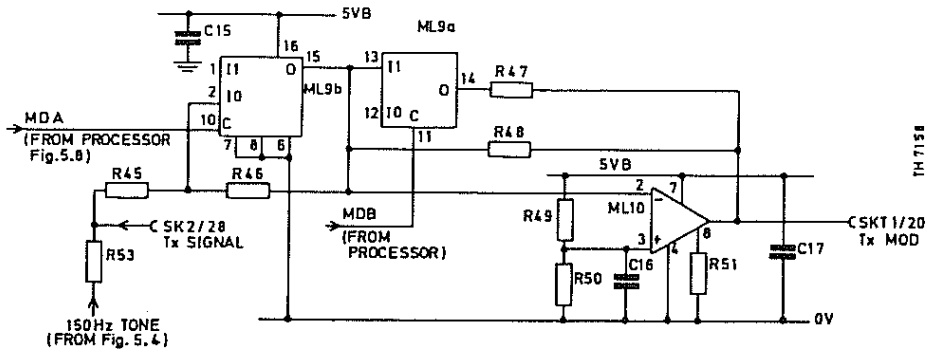


Fig 5.12 Transmit Modulation Buffer Amp

53 Because of the higher percentage bandwidth of modulation at lower transmit frequencies, the processor controls the gain. which can be one of four values, all close to unity. MDA from the processor (ML11, pin 19) controls switch ML9b which switches the TX SIGNAL route to the op amp through R46 or bypasses R46, and MDB (ML12, pin 19) controls switch ML9c which switches R47 in/out of the feedback route. The processor selects the particular switch combination according to information stored in its program, and, in the case of the PRM4515U, operating in the UHF band, only one gain is required.

FUNCTIONAL TESTS AND ALIGNMENT

54 Functional tests and alignment procedures for the Control Board are detailed in Table 5. There is very little alignment: adjustments can be made only in tests 1 and 2. The other tests check correct working of various parts of the circuit and can therefore be used to identify the source of a fault, and to confirm correct operation after a repair.

55 For the tests, operate the Control Board with the remaining parts of a known-working PRM4515U. To allow access to all parts of the board, connect the Transceiver Board to the Control Board via Extender Cable TJ2013, and connect the Crypto Board to the Control Board via Extender Cable TJ2085. Apply a 10 V (nominal) supply to the battery terminals of the PRM4515U, using Battery Adaptor TJ2017 (ensure correct polarity).

56 Set the unit to Clear mode and channel 0, with the OFF/Volume switch at position 1 (first ON position), unless otherwise instructed in the procedures.

TYPICAL VOLTAGES AND WAVEFORMS

57 Typical voltages and waveforms are shown in Table 6. The board under test is set-up as for the functional tests (Para. 55), with access available to all parts and power connected. No other external inputs are used for the static tests.

58 Set the unit to Channel 0 and noise-on (OFF/Volume switch set to position 7).

59 If a crypto module is not fitted in the unit, the Secure mode tests are not necessary.

EQUIPMENT REQUIRED FOR BOARD TESTS

60 (1) DC Power Supply

Voltage	:	0 to 30 V
Current	:	1 A
Example	:	Farnell L30-2

(2) Oscilloscope

Range	:	200 MHz
Impedance	:	1 M ohm
Example Plus a 100 MΩ probe	:	Hewlett Packard 1715A

(3) AF Signal Generator, Two-tone

Range	:	0 to 10 kHz
Output Voltage	:	0 to 20 V dc
Current	:	0 to 10 mA
Example	:	Racal-Dana 9083

(4) Digital Multimeter

Range	:	0 to 5 V rms ac 0 to 20 V dc
Current	:	0 to 10 mA
Example	:	Solartron 7050

(5) Analogue Multimeter

Ranges	:	1 A, 10 V
Example	:	Avometer Model 8

(6) Power Meter (Dummy Load)

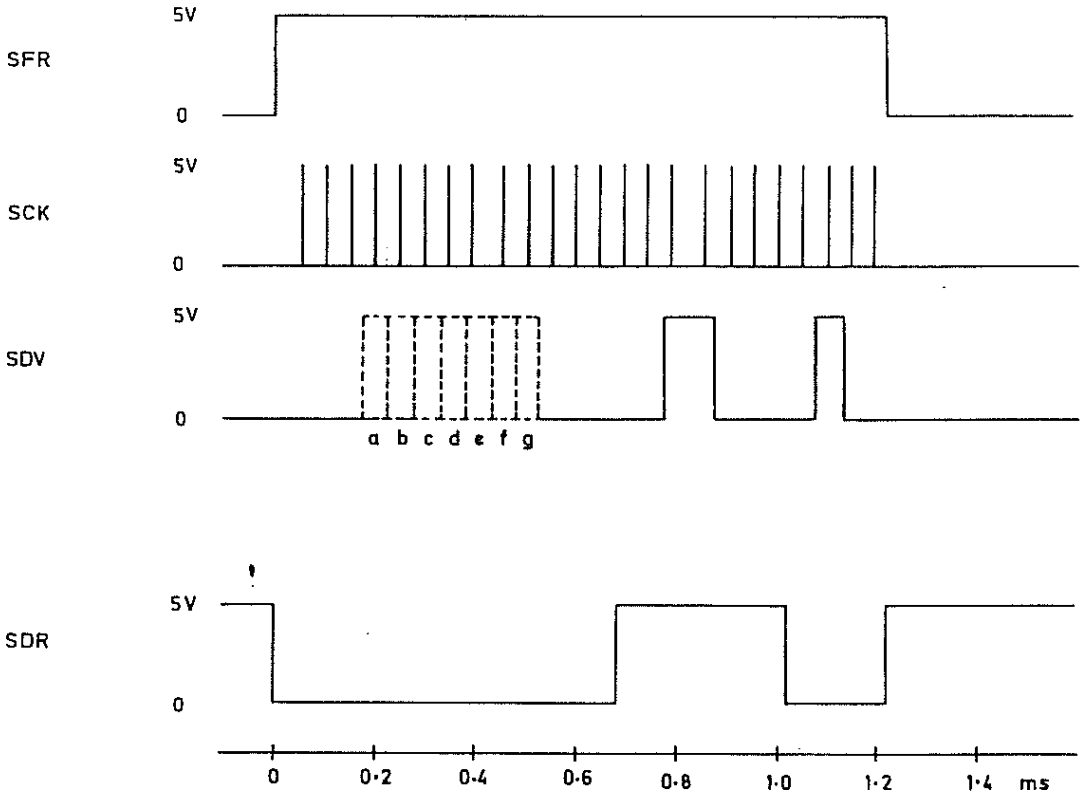
Example : Dymar 2081/100

(7) Test Aids

Extender Cable, 20-way, TJ2013
Extender Cable, 32-way, TJ2085
Audio Interface Jig BCC, TJ1117 (41117-100-10)
Battery Adaptor, TJ2017
Adjustment Tool, 993197EQ
TNC/BNC Adaptor, 993186EQ

(8) Ancillaries

Fill Gun, MA4083B



THE DIAGRAM SHOWS TIMING FOR SYNTHESISER DATA FOR FO + 0.075 MHz RECEIVE

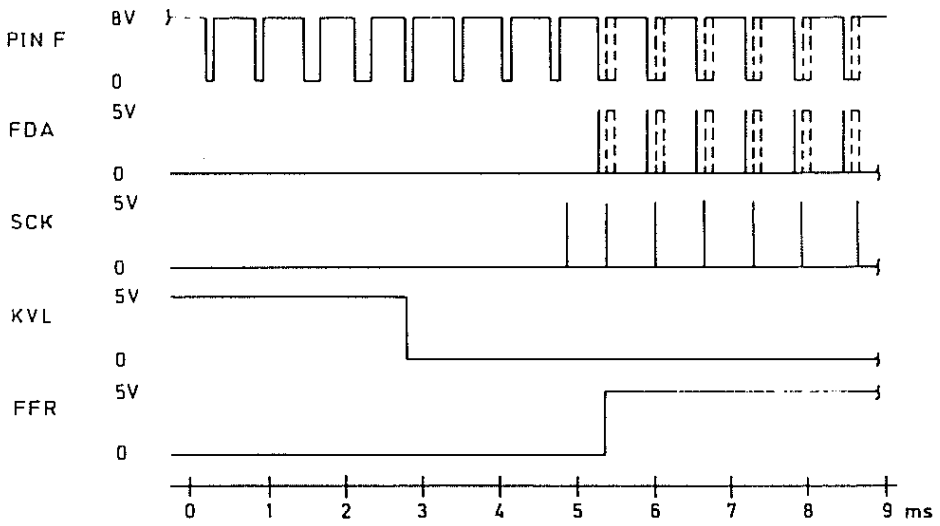
FO IS THE LOWEST FREQUENCY USED BY THE UUT.

THE TABLE SHOWS THE BIT PATTERN (a b c d e f g) APPLICABLE TO THE PARTICULAR CHANNEL 0 (FO + 0.075) USED BY THE UUT. (REF TABLE 5, TEST 20·2)

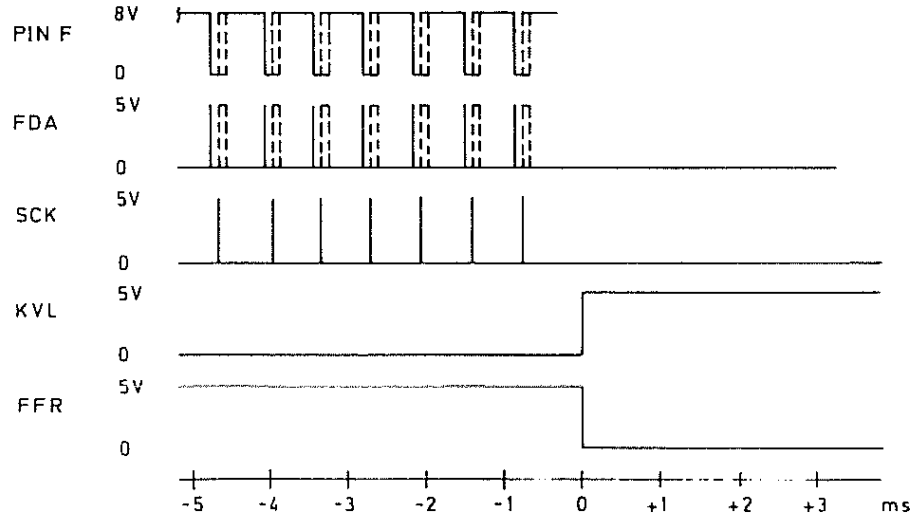
RECEIVE FREQUENCY	BIT PATTERN						
	A	B	C	D	E	F	G
403·075	0	1	1	1	1	0	1
407·075	1	1	1	1	1	0	1
411·075	0	0	0	0	0	1	1
415·075	1	0	0	0	0	1	1
419·075	0	1	0	0	0	1	1
423·075	1	1	0	0	0	1	1
427·075	0	0	1	0	0	1	1
431·075	1	0	1	0	0	1	1
435·075	0	1	1	0	0	1	1
439·075	1	1	1	0	0	1	1
443·075	0	0	0	1	0	1	1
447·075	1	0	0	1	0	1	1
451·075	0	1	0	1	0	1	1

Synthesiser Data : Timing Diagram

Fig. 5.17



Start of Fill Data: Timing Diagram Fig.5.18



End of Fill Data: Timing Diagram Fig.5.19

TABLE 4

Interboard Connector Listing

Pin	I/O	Signal
SK1 (To/from Transceiver Board)		
1		-
2		-
3	O	CTX. Transmit Control.
4	O	10 V Batt.
5		0 V.
6		0 V.
7	O	MAB. Crypto module absent.
8	O	SDV. Synthesiser variable divisor.
9	O	SFR. Synthesiser data frame.
10	O	8VB.
11	O	5VB.
12	O	SDR. Synthesiser reference divisor (and initialise register output enable).
13	I	OOL. Out of lock.
14	O	SCK. Synthesiser (and initialise register) clock.
15	O	SYN. Synthesiser power control.+
16	O	PA CON. Power amplifier control.+
17	O	10 V Batt.
18	I	IDA. Initialise data.
19	I	RX SG. Received signal (demodulated).
20	O	TX MOD. Transmit signal (modulated).
SK2 (To/from Crypto Board)		
1	I	FLA. Fixed-level audio select.
2	I	CRA. Crypto alarm.
3	O	RAD. Received signal (demodulated) for processing by Crypto Board.
4		FAIL.
5	I	MAB. Crypto module absent.
6	I	TON. Crypto transmitting.
7	I	RX AUD. Received signal processed by Crypto Board.
8	O	CTF. Transversal filter power control.
9	O	ZER. Zeroise (erase codes).
10		0 V.
11		8VB.
12	I	DSQ. Digital squelch.
13	O	CTX. Transmit control.
14		10 V Batt.

+ Not used on PRM4515U

TABLE 4 (continued)

Pin	I/O	Signal
15	O	PIN A. Mic/data/FLA program signal.
16		5VB.
17	O	SEC. Secure select.
18	O	XMT. Transmit control.
19	O	KVL)
20	O	KVH) Cipher code select (KVH not used)
21	O	CAF. Audio filter power control.
22	O	WIB. Wideband select.
23		-
24		O V.
25	O	CPS. Crypto clock generator power control. Held high.
26	O	SCK. Clock for crypto fill.
27		-
28	I	TX SIG. Signal for transmission.
29	O	FDA. Crypto fill data.
30	O	FFR. Crypto fill frame.
31	I	WB AUD. Received wideband signal (switched on Crypto Board).
32	O	WHI. Whisper select.

TABLE 5

Functional Tests and Alignment

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
1.1	8 volt regulator & on/off switching	Clear, Ch 0, Vol Sw posn 0.	10.0V on battery connector	SK1/10 (8VB)	0V±0.5V	
1.2		Vol Sw posn 1			8V±10mV	Adjust R6
2	5 volt regulator	Clear, Ch 0, Vol Sw posn 1		SK1/11 (5VB)	5.2V±10mV	Adjust R13
3.1	Supply out on Pin C (Audio socket)	As Test 2		SK6/C (Pin C)	10±0.1V	
3.2	Current limit		50 ohm load		100±30mA	Ensure that this limit applies even with a short circuit on output (as in Test 3.3)
3.3			Avometer (100mA) load on Pin C		100±30mA	
4.1	Supply via Pin C	As Test 2	10V dc at Pin C	Battery connector	10±0.1V	Remove normal supply from battery connector
4.2	Overvoltage Pin C		Up to 16.6V at Pin C		0V±0.5V for 15.6±1V at Pin C	Increase supply at Pin C until battery connector voltage falls to zero
5.1	Fail Generator	As Test 2		SK2/4 (Fail)	0V±0.5V	
5.2		Sec A			5V±0.5V	(Mode sw posn 2 (A))

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
6.1	Reset	As Test 2	4.5V at ML7/40	ML7/1 (Reset)	<1V	Reduce supply voltage at battery terminal until ML7/40 is 4.5V, and check ML7/1 limits
6.2			5.0V at ML7/40		>3.8V	Increase supply voltage until ML7/40 is 5.0V, and check ML7/1 limits
7.1	Whisper	Vol Sw posn 1		SK2/32 (WHI)	5V±0.5V	
7.2		2			5V±0.5V	
7.3		3			0V±0.5V	
7.4	CNO	8		ML7/19 (CNO)	5V±0.5V	
7.5		7			5V±0.5V	
7.6		3			0V±0.5V	
8.1	PTT	As Test 2	0V at Pin F	ML7/24 (SDI)	0V±0.5V	
8.2			Pin F open-circuit		5V±0.5V	
9.1	Volume Control	Vol Sw posn 1	Apply RF signal to SK1 at Rx frequency with 1kHz modulation, 4kHz deviation, and 150Hz modulation, 750Hz deviation	Pin D with 300Ω	0.12±0.05V rms	
9.2		2			0.23±0.08V rms	
9.3		3			0.46±0.15V rms	
9.4		4			0.92±0.15V rms	
9.5		5			2.0 ±0.3V rms	
9.6		6			3.0 ±0.5V rms	Clipped
9.7		7			0.46±0.15V rms	
9.8		8			3.0 ±0.5V rms	Clipped
9.9	FLA	3	As above, plus 1mA into Pin A		2.0±0.3V rms	

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
10	Modulation buffer	Clear, Tx (Pin F at 0V)		SK1/20 (TxMod)	150Hz sinewave, 0.09±0.01V rms	
11	CNO	Clr, Ch 0, Vol Sw posn 7		SK2/21(CAF)	0V±0.5V	
				SK1/15(SYN)	0V±0.5V	
				Pin G	5V±0.5V	Into 4k7Ω load
				Pin D	Noise	
12.1	MOA/MOB	As Test 2		SK1/15(SYN)	0V/5V toggling	
				SK2/25(CPS)	5V±0.5V	
				SK2/17(SEC)	5V±0.5V	
12.2		Sec B		SK1/15(SYN)	0V/5V toggling	(Mode sw posn 3(B))
				SK2/19(KVL)	5V±0.5V	
				SK2/25(CPS)	5V±0.5V	
				SK2/17(SEC)	0V±0.5V	
13	OOL	As Test 2	Touch L9 (to stop Rx VCO)	SK1/15(SYN)	0V±0.5V	
				SK2/13(CTX)	0V±0.5V	
				SK2/21(CAF)	0V±0.5V	
				Pin G	5V±0.5V	Into 4k7Ω
				Pin D	1kHz/2kHz	(two-tone alarm)
14	Rx WIB audio (audio amp)	As Test 2	Apply RF signal to SK1, at Rx frequency with 1kHz modulation, 5kHz deviation. Also, 1mA into Pin B.	Pin D	1.4±0.3V rms	
15	WIB	As Test 2	1mA into pin B	SK1/15(SYN)	0V±0.5V	
				SK2/21(CAF)	0V±0.5V	
				SK2/25(CPS)	5V±0.5V	
16	Zeroise gating	Zeroise		SK2/9(ZER)	0V±0.5V	(Mode sw posn 0(Z))

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
17	CRA	Zeroise		SK2/2	5V±0.5V	Reload cipher codes after test
				Pin G	5V±0.5V	
				Pin D	1kHz	
18	Clear PTT	As Test 2	OV at Pin F	SK1/15(SYN)	OV±0.5V	1kHz pips audible at handset
				SK2/13(CTX)	OV±0.5V	
				SK2/21(CAF)	OV±0.5V	
				Pin G	5V±0.5V into 4k7Ω load	
19.1	Secure PTT and TON	Sec A	OV at Pin F (PTT)	SK1/15(SYN)	OV±0.5V	No pips at handset
				SK2/13(CTX)	OV±0.5V	
				SK2/21(CAF)	OV±0.5V	
				SK2/17(SEC)	5V±0.5V	
				SK2/8(CTF)	5V±0.5V	
				SK2/18(XMT)	5V±0.5V	
19.2			Pin F open-circuit	SK1/15(SYN)	OV/5V toggling	
				SK2/13(CTX)	5V±0.5V	
				SK2/21(CAF)	5V±0.5V	
				SK2/17(SEC)	OV±0.5V	
				SK2/8(CTF)	OV±0.5V	
				SK2/18(XMT)	OV±0.5V	
20.1	PWM channel data	As Test 2	PWM channel and frequency data, from MA4083B, at Pin F. (Use frequencies as shown in right-hand columns of this table)	Ch0:F0+0.075MHz Ch1:F0+2.300MHz Ch2:F0+4.525MHz Ch3:F0+6.700MHz Ch4:F0+8.950MHz	Ch5:F0+11.1875MHz Ch6:F0+12.4125MHz Ch7:F0+15.6250MHz Ch8:F0+17.850MHz Ch9:F0+19.9125MHz	
				F0 is lowest frequency used by UUT, indicated by a letter code:		
				A:403MHz B:407MHz C:411MHz D:415MHz	E:419MHz F:423MHz G:427MHz H:431MHz	J:435MHz K:439MHz L:443MHz M:447MHz N:451MHz

1N4 MHz steps from 403(A) to 451(N)

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
20.2	Synthesiser data	Vol Sw posn 7		SK1/14(SCK) SK1/12(SDR) SK1/8(SDV) SK1/9(SFR)	See Fig 5.17	Step Channel switch from 0 to 9. At each position check that a new frequency word is sent to the synthesiser. Also check that on return to 0, SDV, SDR, SCK, SFR are as shown in Fig 5.17.
21	Fill data	Sec B	PWM data: 00110000 10000010 at Pin F	Pin F SK2/26(SCK) SK2/39(FFR) SK2/29(FDA) SK2/19(KVL)	See Figs 5.18 and 5.19	

TABLE 7

Static Reference Voltages
(No External Inputs)

	Clear, Rx, Noise-On (Vol Sw posn 7)			Clear, Tx			Sec A, Tx		
	E(s)	B(g)	C(d)	E(s)	B(g)	C(d)	E(s)	B(g)	C(d)
TR1	10	9.4	6.6	-	-	-	-	-	-
TR2	10	6.6	8.0	-	-	-	-	-	-
TR3	0	0.6	0	-	-	-	-	-	-
TR4	6.6	7.2	9.4	-	-	-	-	-	-
TR5	8.0	4.8	5.0	-	-	-	-	-	-
TR6	5.0	6.6	0	-	-	-	-	-	-
TR7	10	10	0	-	-	-	-	-	-
TR8	10	0	10	-	-	-	-	-	-
TR9	10	0	10	-	-	-	-	-	-
TR10	10	10	0	-	-	-	-	-	-
TR11	5.2	5.0	0	5.0	4.3	4.6	5.0	4.3	4.6
TR12	0	5.0	0	-	-	-	-	-	-
TR13	8.0	0	8.0	-	-	-	-	-	-
TR14	0	0	5.0	-	-	-	-	-	-
TR15	0	0	7.7	0	0	0.1	0	0	0.1
TR16	5	7.4	0	5.0	4.4	5.0	5.0	4.4	5.0
TR17	0.6	0	0	-	-	-	-	-	-
TR18	0.6	0	0	0.6	0	0	5.0	5.0	0
TR19	10	0	10	10	0	10	10	8.7	< 2
TR20	0	5.0	0	0	5.2	0	0	0	8.7
TR21	8.8	10	10	8.5	9.6	9.6	< 2	< 2	< 2
TR22	0	0	5.0	-	-	-	-	-	-

Where - is shown instead of a number, there is no change from Clear, Rx, Noise-On.

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
1	1	0	-	-	-					Note: Where - is shown instead of a number, there is no change from Clear, N-On
	2	2.3	-	-	-					
	3	2.3	-	-	-					
	4	0	-	-	-					
	5	0	-	-	-					
	6	5.0	-	-	-					
	7	8.0	-	-	-					
	8	7.4	-	-	-					
2	1	0	-	-	-					
	2	2.3	-	-	-					
	3	2.3	-	-	-					
	4	0	-	-	-					
	5	0	-	-	-					
	6	4.5	-	-	-					
	7	5.0	-	-	-					
	8	4.45	-	-	-					
3	1	0	-	-	-					
	2	0	-	-	-					
	3	1.7	-	-	-					
	4	0	-	-	-					
	5	0	-	-	-					
	6	4.4	-	-	-					
	7	5.0	-	-	-					
	8	4.45	-	-	-					
4	1	L	H	H	-					Note: L = 0 V ± 0.5 V H = 5.2 V ± 0.5 V
	2	L	L	L	-					
	3	L	L	L	-					
	4	H	H	H	-					
	5	H	H	H	-					
	6	H	H	H	-					
	7	L	L	L	-					
	8	L	L	L	-					
	9	L	L	L	-					
	10	L	L	L	-					
	11	L	L	L	-					
	12	L	L	L	-					
	13	L	L	L	-					
	14	H	H	H	-					
5	1	L	H	H	-					
	2	L	H	H	-					
	3	H	L	L	-					
	4	H	H	H	-					
	5	L	H	H	-					
	6	H	L	L	-					
	7	L	L	L	-					

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
	8	H	H	H	-					Note: Where - is shown instead of a number, there is no change from Clear, N-On
	9	H	H	H	-					
	10	L	L	L	-					
	11	H	H	H	-					
	12	L	L	L	-					
	*13	H	H	H	-					Use 10 MΩ probe for pins marked *
	14	H	H	H	-					
6	1	L	L	L	-					
	2	L	L	L	-					
	3	H	H	H	-					
	4	L	L	H	-					
	5	H	H	L	-					
	6	L	L	L	-					
	7	L	L	L	-					
	8	H	L	L	-					
	9	H	L	L	-					
	10	L	H	H	-					
	11	L	L	L	-					
	12	L	L	L	-					
	*13	H	H	H	-					
	14	H	H	H	-					
7	1	H	H	H	-					
	2	H	H	H	-					
	3	L	L	L	-					
	4	L	L	L	-					
	5	L	L	L	-					
	6	L	L	L	-					
	7	L	L	L	-					
	8	L	L	L	-					
	9	L	L	L	-					
	10	L	L	L	-					
	11	L	L	L	-					
	12	L	L	L	-					
	13	L	L	L	-					
	14	L	L	L	-					
	15	L	L	L	-					
	*16	H	H	L	-					
	*17	H	H	H	-					
	*18	H	H	H	-					
	19	H	H	H	-					
	20	L	L	L	-					
	21	L	L	L	-					
	22	L	L	L	-					
	23	H	L	L	-					
	24	H	L	L	-					
	25	L	L	L	-					

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
	26	L	L	L	-					Note: Where - is shown instead of a number, there is no change from Clear, N-On
	27	L	AC	L	-		Fig 1			
	28	H	H	H	-					
	29	L	L	L	-					
	30	L	L	L	-					
	31	AC	AC	L	-	Fig 2	Fig 3			
	32	L	L	L	-					
	33	L	L	L	-					
	34	L	L	H	-					
	35	H	H	H	-					
	36	L	L	L	-					
	37	L	L	L	-					
	38	AC	AC	AC	-	Fig 4	Fig 4	Fig 4		
	39	2.5	2.5	2.5	-					
	40	5.2	5.2	5.2	-					
8	1	0	0	0	-					
	2	0	0	0	-					
	3	0	0	0	-					
	4	0	0	0	-					
	5	0	0	0	-					
	6	0	0	0	-					
	7	0	0	0	-					
	8	0	5.2	0	-					
9	1	0	0	0	-					
	2	2.0	2.0	2.0	-					
	3	2.5	0	0	-	Fig 5	Fig 6			
	4	2.5	2.0	0	-	Fig 5	Fig 6			
	5	0	2.2	0	-		Fig 6			

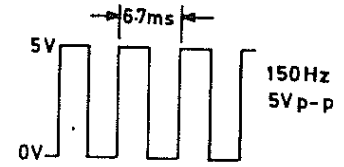


Fig 1

Fig 2

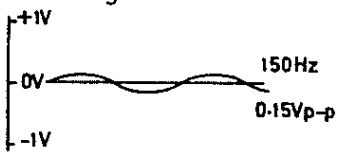


Fig 3

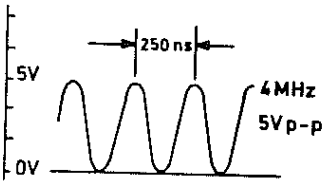


Fig 4

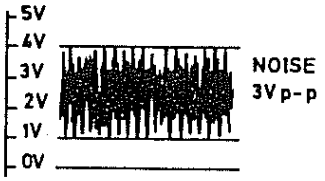


Fig 5

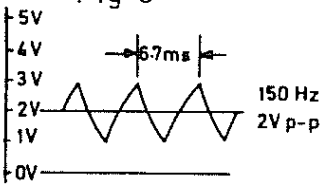


Fig 6

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
	6	0	0	0	-					
	7	0	0	0	-					
	8	0	0	0						
	9	5	0	0	-					
	10	0	0	0	-					
	11	0	0	0	-					
	12	1.2	1.2	1.7	-	Fig 7	Fig 8	Fig 9		
	13	2.0	2.0	2.0	-					
	14	1.2	1.2	1.7	-	Fig 7	Fig 8	Fig 9		
	15	2.0	2.0	2.0	-					
	16	5	5	5	-					
10	1	0	0	0	-					
	2	2.0	2.0	2.0	-					
	3	2.0	2.0	2.0	-					
	4	0	0	0	-					
	5	0	0	0	-					
	6	2.0	2.0	2.7	-	Fig10	Fig11	Fig12		
	7	5	5	5	-					
	8	4.5	4.5	4.5	-					

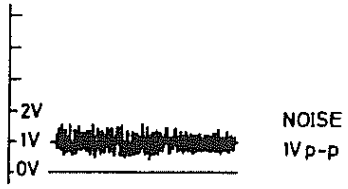


Fig 7

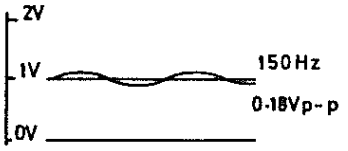


Fig 8

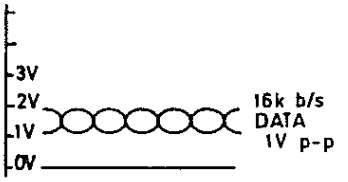


Fig 9

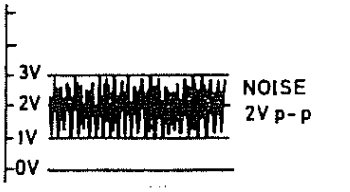


Fig 10

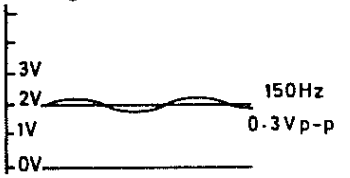


Fig 11

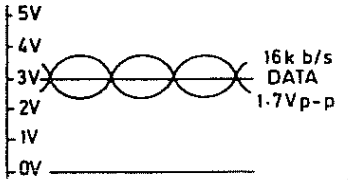


Fig 12

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
11	1	L	L	L	-					Note: Where - is shown instead of a number, there is no change from Clear, N-On
	2	H	H	L	-					
	3	L	L	L	-					
	4	L	L	L	-					
	5	L	L	H	-					
	6	H	H	L	-					
	7	L	L	L	-					
	8	L	L	L	-					
	9	L	L	L	-					
	10	L	L	L	-					
	11	L	L	L	-					
	12	H	L	L	-					
	*13	H	H	L	-					
	*14	H	H	H	-					
	15	L	L	L	-					
	16	L	L	L	-					
	*17	H	H	H	-					
	18	H	H	H	-					
	19	L	L	L	-					
	20	H	H	H	-					
12	1	L	L	L	-					
	2	L	L	L	-					
	3	L	L	L	-					
	4	L	L	L	-					
	5	H	H	H	-					
	6	H	H	L	-					
	7	L	L	L	-					
	8	L	L	L	-					
	9	L	L	L	-					
	10	L	L	L	-					
	11	L	L	L	-					
	12	H	H	L	-					
	*13	H	H	L	-					
	*14	H	H	H	-					
	15	L	L	H	-					
	16	L	H	L	-					
	*17	H	H	H	-					
	18	H	H	H	-					
	19	L	L	L	-					
	20	H	H	H	-					
14	1	0	0	0	-					
	2	2.0	2.5	0.7	-	Fig13	Fig14			
	3	1.5	1.7	0	-	Fig13	Fig15			
	4	0	0	0	-					
	5	0	0	0	-					
	6	2.0	2.5	0.7	-	Fig13	Fig14			
	7	5	5	0	-					
	8	4.5	4.5	0	-					

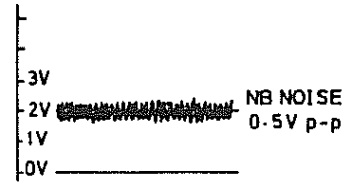


Fig 13

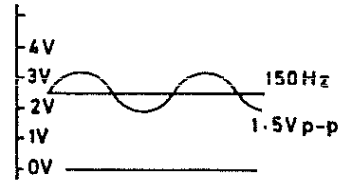


Fig 14

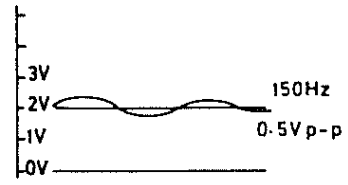


Fig 15

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
15	1	0	0.2	0	-	Fig16	Fig17			Note: Where - is shown instead of a number, there is no change from Clear, N-On
	2	1.8	2.5	0.7	-		Fig17			
	3	1.8	2.5	0.7	-	Fig18	Fig19			
	4	0	0	0	-					
	5	0	0	0	-					
	6	0	0	0	-					
	7	0	0	0	-					
	8	5	0	0	-					
16	*1	4.0	4.0	0	-					
	*2	3.5	3.5	3.5	-	Fig20				
	*3	3.5	3.5	0	-	Fig20				
	*4	4.0	4.0	0	-					
	*5	4.0	4.0	0	-					
	6	0	0	0	-					
	7	0	0	0	-					
	8	0	0	0	-					
	9	5	5	5	-					
	10	5	5	5	-					
	11	0	0	0	-					
	*12	3.5	3.5	0	-					
	*13	3.5	3.5	0	-					
	*14	4.0	4.0	0	-					
	*15	4.0	4.0	0	-					
	16	5	5	5	-					

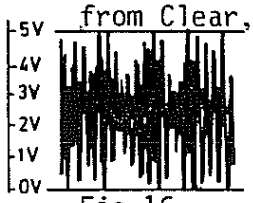


Fig 16

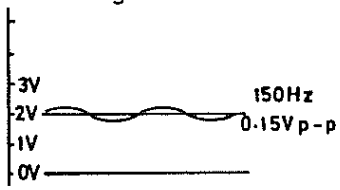


Fig 17

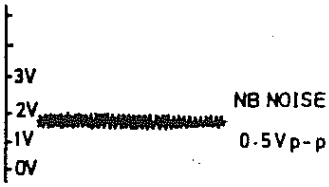


Fig 18

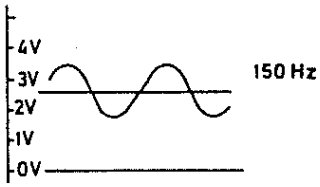


Fig 19

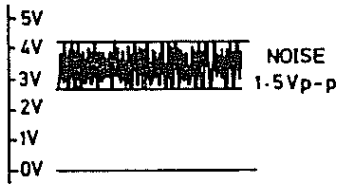
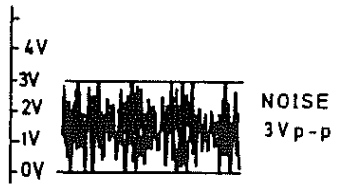
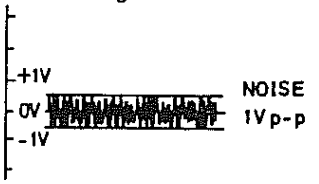
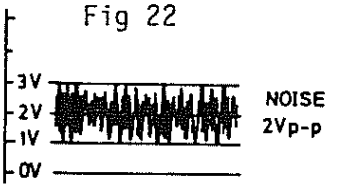


Fig 20

ML	Pin	D.C. Volts				A.C. Volts				A.C. Waveforms and Notes
		Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	Clear N-On	Clear Tx	Sec A Tx	Sec A N-On	
17	1	1.5	0	0	-	Fig21				 Fig 21
	2	4.0	4.0	0	-					
	3	0	0	0	-	Fig22				
	4	0	0	0	-	Fig22				
	5	0	0	0	-	Fig22				
	6	0	0	0	-					
	7	0	0	0	-					
	8	0	0	0	-					
	9	1.3	0	0	-					 Fig 22
	10	0	0	0	-					
	11	0	0	0	-					
	12	2.0	0	0	-	Fig23				
	13	0	0	0	-					
	14	2.0	0	0	-	Fig23				
	15	4.0	4.0	0	-					
	16	5	5	5	-					
18	1	3.6	3.6	3.6	-					 Fig 23
	2	4.0	4.0	0	-					
	3	0	0	0	-					
	4	4.0	4.0	0	-	Fig23				
	5	8.8	8.8	0.6	-					
	6	0	0	0	-					
	7	8.1	7.8	0	-					
	8	0	0	0	-					

CHAPTER 6

CRYPTO BOARD

CONTENTS

	Page
INTRODUCTION	6-1
BRIEF DESCRIPTION	6-1
Power	6-1
Transmit Mode	6-1
Standby/Receive Mode	6-2
Loading and Erasing Cipher Codes	6-4
DETAILED DESCRIPTION	6-5
5V Supply Isolator	6-5
Vogad	6-5
Audio Filter	6-6
Codec	6-7
Clock Generator	6-8
Slicer	6-9
Clock Recovery	6-10
Crypto (and Reversals Control)	6-10
Transversal Filter	6-12
FUNCTIONAL TESTS AND ALIGNMENT	
TYPICAL VOLTAGES AND WAVEFORMS	
EQUIPMENT REQUIRED FOR TESTS	

TABLES

Table No.

1	Interboard Connector Listing
2	Power Rail Tests
3	Alignment
4	Clear Transmit Tests
5	Secure Transmit Tests
6	Clear Receive Tests
7	Secure Receive Tests
8	Static Reference Voltages

ILLUSTRATIONS

Fig. No.

6.1	Transmit Signal Routeing
6.2	Crypto Board: Block Diagram
6.3	Receive Signal Routeing
6.4	5V Supply Isolator
6.5	Vogad
6.6	Audio Filter
6.7	Codec
6.8	Clock Generator, Slicer and Clock Recovery
6.9	Crypto and Reversals Control
6.10	Transversal Filter
6.11	Crypto Board: Circuit
6.12	Crypto Board: Layout

CHAPTER 6

CRYPTO BOARD

INTRODUCTION

1 The Crypto Board contains a speech security circuit and transmit audio processing circuit.

BRIEF DESCRIPTION (Fig. 6.2, 6.11)

Power

2 The board is powered by the 5VB (CONT) and 8VB (CONT) 'black' supplies, which are present when the unit is switched-on. The supply isolator provides a separate 5VR (CONT) 'red' supply for use by the parts of the circuit that process clear audio signals. This prevents high audio currents from modulating the 'black' supply rails.

3 When the 5VB (CONT) and 8VB (CONT) supplies are removed, the 10V BATT battery supply provides power for the crypto module, which must have power to store the cipher codes. If the battery supply is removed, a charged capacitor on the board provides sufficient power to retain the codes for at least 15 minutes.

4 Most of the circuits on the board are powered only when they are required for a particular operation. 5VB-CPS provides power for the clock generator and Rx signal slicer, used in secure operation, and 5VB-CTF provides power for the transversal filter, used in secure transmission. The control signal CTX switches power from 5VR to the vogad, used in transmit operation, and CAF switches power from 5VR to the audio filter and codec, used in narrowband operation.

Transmit Mode (Fig. 6.1)

5 The MIC audio input signal goes to a voice operated gain adjusting device (vogad) which converts it to a constant level signal. The vogad's output goes via the audio bandpass filter to the codec, which converts it to the digital form required by the crypto module.

6 The crypto module, on receipt of XMT, carries-out a self check. If there is a fault (eg. it has no cipher codes),it outputs an alarm signal (CRA). If the test is successful, the module outputs phase reversals on the transmit line (TCT) so that the receiving unit can synchronise its data bit rate clock. The module adds a sync code so that the receiving unit can set its decryption circuits correctly to decrypt the message data, then it encrypts the data for transmission (TPT). The encrypted output (TCT) goes to a transversal filter, which converts it from squarewave form to a sinusoidal form that is more suitable for transmission, then it leaves the board as TX SIG.

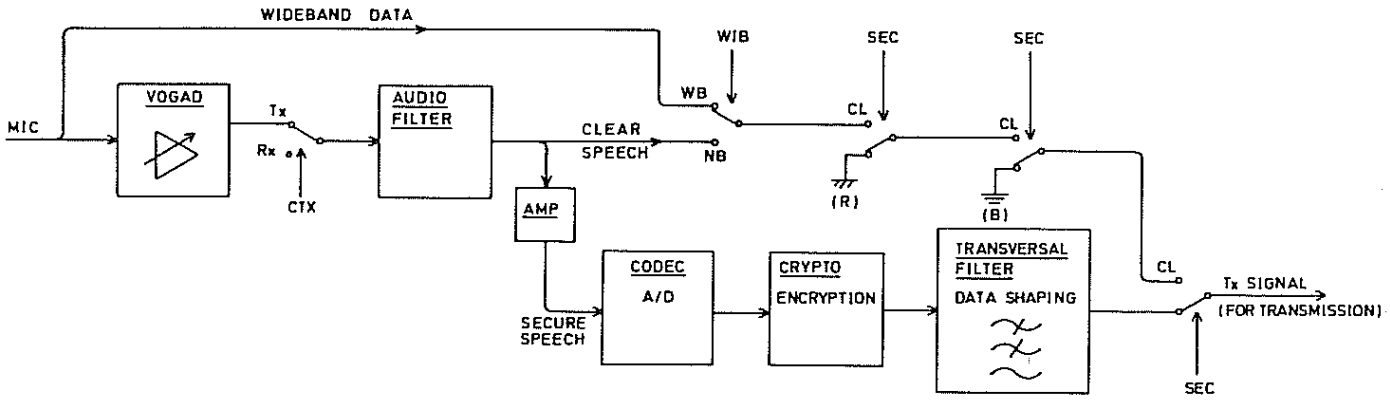


Fig 6.1 Transmit Signal Routeing

7 Clear voice transmit signals go via the vogad and audio filter (as above), bypass the crypto and go out as TX SIG. An arrangement of three switches ensures that the clear signal is kept well clear of the encrypted transmit signal during secure operation.

8 When the unit is in wideband mode, transmit signals go straight through the board and out as TX SIG.

Standby/Receive Mode (Fig. 6.3)

9 Basically. when the 5VB (CONT) and 8VB (CONT) supplies are present, and the unit is not transmitting, it is ready to receive. Sinusoidal received data, RX SIG, goes to a slicer which converts it to a squarewave form suitable for use by the clock recovery and decryption circuits. When the clock recovery circuit detects the presence of a 16k bit/sec signal, it outputs a DSQ (Data Squelch) signal to indicate that valid data is arriving, and locks the board's own data bit rate clock signal to the phase of the incoming data stream. As a result of Data Squelch, power is applied to other necessary parts of the circuit. (The slicer and clock generator are powered by 5VB-CPS, so the presence of secure Rx data can be detected only when 5VB-CPS is present).

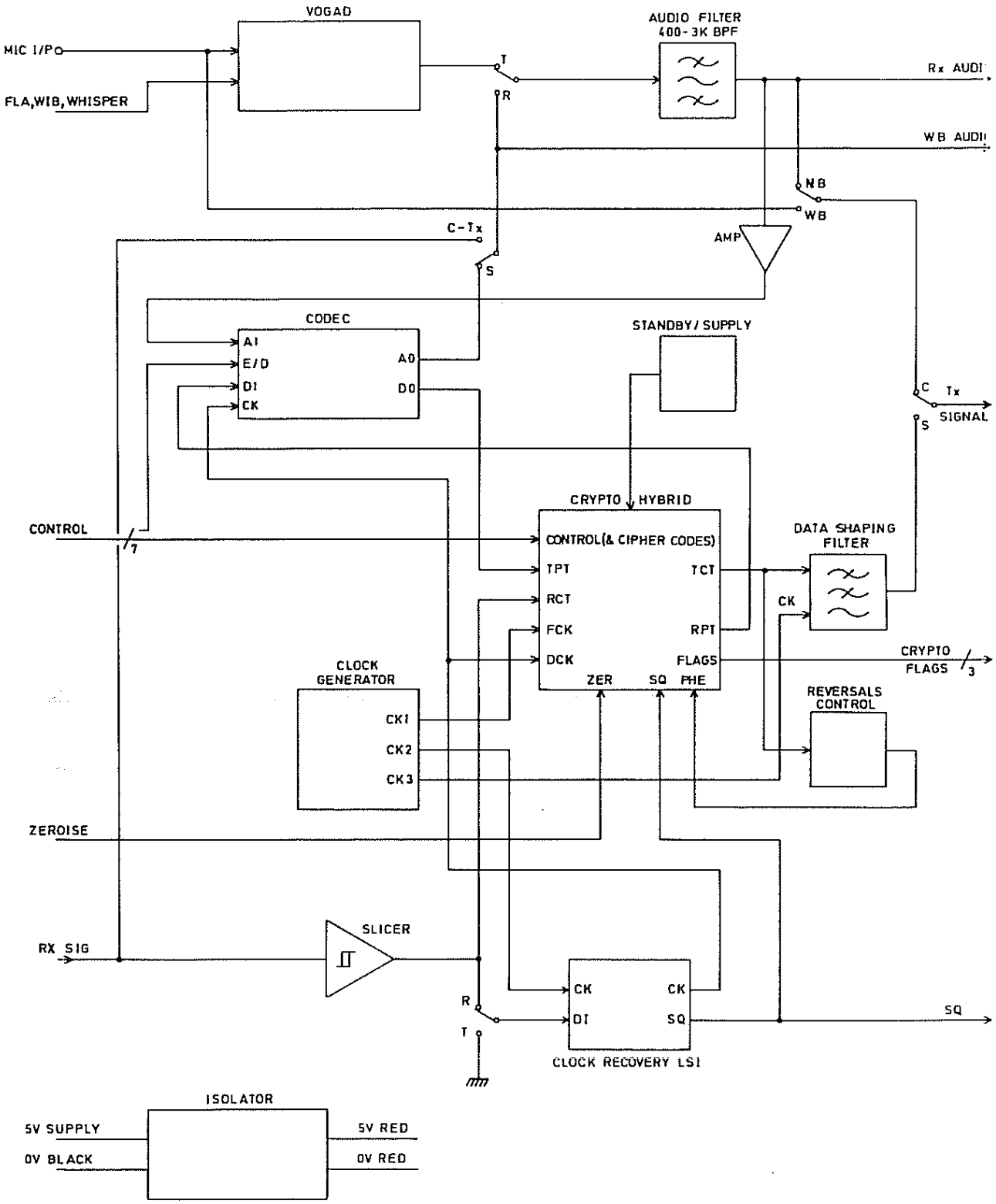


Fig 6.2 Crypto Board: Block Diagram

10 On receipt of Squelch, the crypto module uses the sync code in the incoming data (RCT) to check that it has the required cipher code and set its circuits ready to decrypt the message data that follows. When ready it outputs a Sync signal and starts to decrypt the data. The decrypted data (RPT) goes to the codec, which converts it into an audio waveform, then via the audio filter, and out as RX AUDIO.

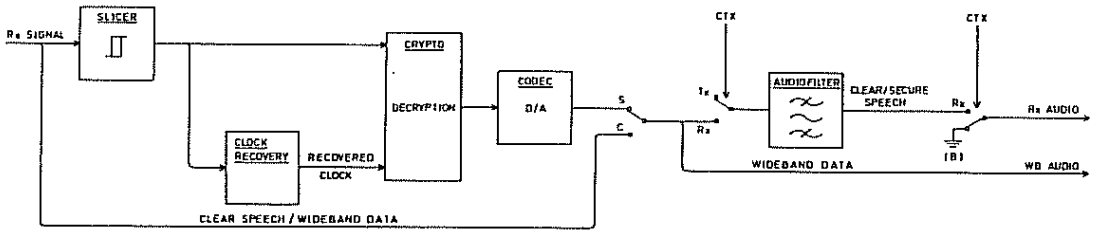


Fig 6.3 Receive Signal Routeing

11 Clear received signals bypass the clock recovery and crypto circuits, and go directly to the audio filter then out as RX AUDIO.

12 When the unit is in wideband mode, received signals go straight through the board and out as WB AUDIO.

Loading and Erasing Cipher Codes

13 The crypto module accepts and stores cipher codes (key variable (KV) data) clocked-in by Fill Clock, when the Frame signal is active. New data overwrites old data in the store. The data is stored until power is completely removed (Para. 3). The ZER (Zeroise) input provides a code erasure facility.

DETAILED DESCRIPTION (Fig 6.11)

5V Supply Isolator (Fig. 6.4)

14 The 5V supply isolator prevents modulation of the unit's 5V supply by the changing current demands of the audio-frequency circuits. The 5VB (CONT) black supply (PL1/16) turns-on transistors TR1, TR2 which switch through the main supply, 8VB (CONT) (PL1/11) to provide the 5VR (CONT) red supply for the audio circuits. All the current refers to reservoir capacitor C3 which acts as a 5.6V battery. The voltage drop across diode D4 holds 5VR (CONT) at 5V, with capacitor C4 acting as an additional reservoir. The capacitors smooth peaks and troughs in the current drawn, so there is a constant flow of current from the 8VB (CONT) supply. R2, R3, C1 act as a filter to isolate the current to the base of TR1.

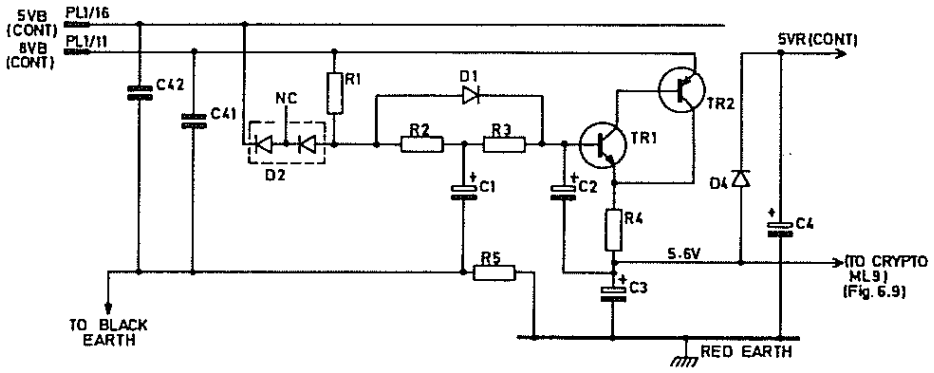


Fig 6.4 5 V Supply Isolator

Vogad (Fig. 6.5)

15 The voice operated gain adjusting device amplifies the MIC signal (PL1/15). Its gain adjusting circuit clips fast peaks and thus maintains the mean level, and its decay time is slow enough to maintain the syllabic content of the speech waveform.

16 When CTX (PL1/13) goes high, the low output from NOR gate ML10a (pin 3) turns on FET TR3, which switches power (5VR-CTX) to the vogad from the 5VR (CONT) rail. The vogad's nominal input is 1mV (rms) from MIC (PL15), which the preamplifier, op amp ML1 plus associated components, amplifies to 2mV.

17 Switches ML2b, ML2c add or subtract resistors in the amplifier's feedback route to suit other inputs. When WHI (Whisper, PL1/32) is high, ML2b adds R15 to the feedback route, so a whisper-level 0.25 mV (rms) signal is amplified to 2mV. When there is 1 mA (plus) fixed level audio on the MIC input, switch ML2c puts R14 in parallel with R13 and thus reduces the resistance in the feedback route such that a 10 mV (rms) signal produces the required 2 mV from the

preamplifier. The FLA signal also leaves the board via PL1/1. When there is 1mA on WIB (PL1/22), FET TR5 turns-on and shorts FLA for wideband operation. The wideband signal from MIC bypasses the vogad and audio filter; WIB switches it via ML5a onto the TX SIG route.

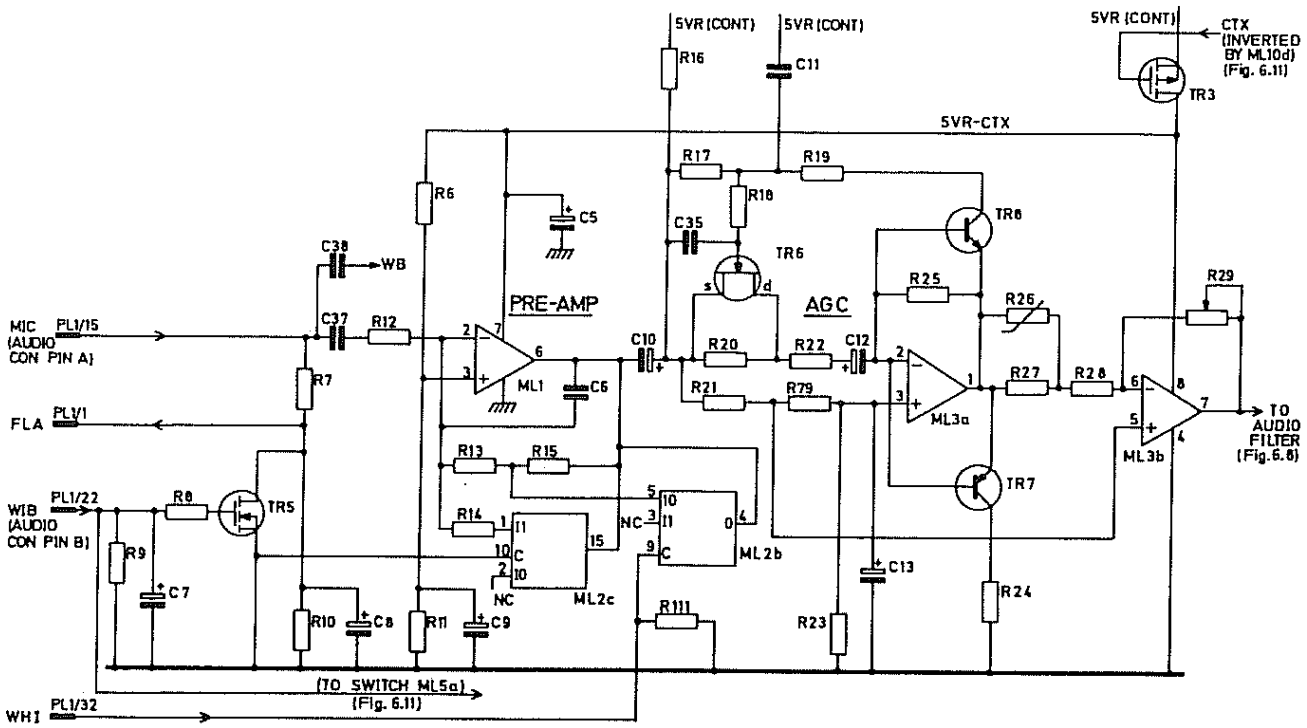


Fig 6.5 Vogad

18 The automatic gain control circuit, op amp ML3a plus associated components, provides a gain of up to 180. Transistors TR8 and TR7 maintain 1.3V peak-to-peak into R27. If the gain goes too high, TR8 turns-on, so FET TR6, which is normally on, turns-off. This switches R20 into the circuit, and the increased input resistance reduces the gain of the amplifier. R19 determines the attack time of the circuit, and R17 determines the decay time. Op amp ML3b, thermister R27, plus associated components provide temperature stability, and potentiometer R29 allows adjustment of the audio output from the vogad circuit.

Audio Filter (Fig 6.6)

19 When CAF (PL1/21) goes low it turns-on FET TR4 which switches power (5VR-CAF) to the audio filter circuit (and codec) from the 5VR (CONT) rail. When CTX (PL 13) is high for a transmit operation, the transmit/receive switch ML2a switches through the output from the vogad to the filter; when CTX is low, the circuit filters the receiver signal prior to its output as RX AUDIO.

20 The low-pass filter removes frequencies above 2.7 kHz; the high-pass filter removes frequencies below 350 Hz, and in particular it notches-out the 150 Hz squelch. For clear voice transmission, the

output from the filters is switched via ML5a by WIB low, and it goes via the clear/secure switches ML5c, ML8c, ML8b as TX SIG (PL1/28). For wideband transmission, WIB high switches the WB signal, which bypasses the vogad and filters, through ML5a instead. In receive operation, the decoded signal from the crypto (via the codec), or the clear received signal, is switched through ML5b (by SEC) to the audio filter, via ML8a (by CTX) and out as RX AUDIO (PL1/7). Wideband received signals bypass the filters (which are switched-off by CAF high) and leave the board as WB AUDIO (PL1/31). 100 ohm resistors (eg. R95) on the outputs act as RF filters to prevent RF signals from entering the board.

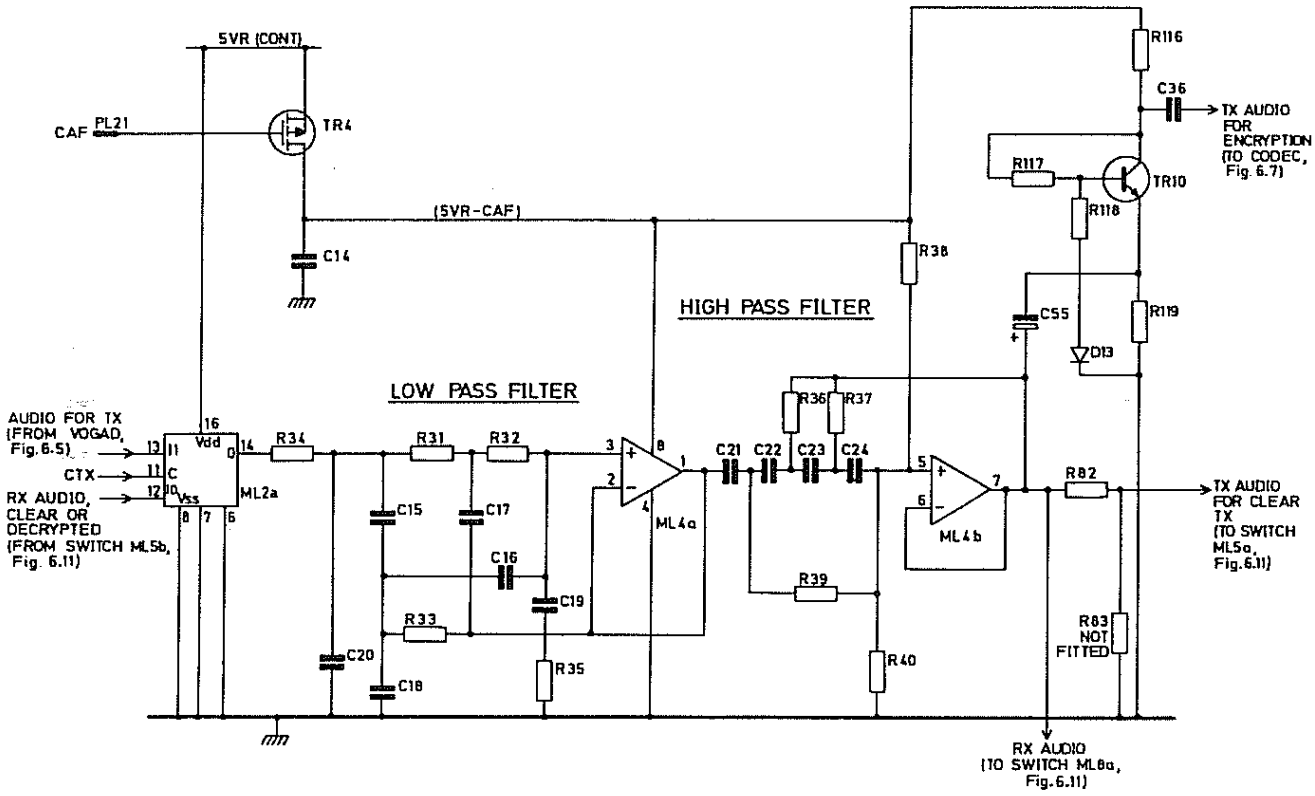


Fig 6.6 Audio Filter

21 For secure transmission, the amplifier circuit that consists of TR10 plus associated components amplifies the 1.3V filtered signal to 3.5V peak-to-peak for use by the codec (and crypto, etc).

Codec (Fig. 6.7)

22 The codec, ML11, is a continuously-variable-slope delta modulator/demodulator. In secure transmit operation, CTX high, inverted to low by NOR gate ML10a, makes the DEC input (pin 10) low, so the codec converts the audio signal at AUD IN (pin 5) to 16k bit/sec digital data, from DIG (pin 14), for the crypto circuit. CKO from

ML14 provides the clock input to CK (pin 9). A low signal to FZ (pin 13) forces an all-zero output and thus mutes the codec, and capacitor C56 provides a start-up reset by muting the codec until the capacitor has charged.

23 In secure receive operation, the signal to DEC is high, so the codec converts the decrypted serial data at DIG IN (pin 12) to (stepped) audio data from AUD OUT (pin 3). The audio output from the codec is filtered by op amp ML12 plus associated components, which smooth the higher steps in the signal and remove digitiser noise. CTX and SEC both low make the output from NOR gate ML10b high to switch the decrypted received signal through ML5b to the audio filter. When SEC is high, RX SIG (clear received data) goes through ML5b instead. When the unit is transmitting, CTX high forces the switch to the clear position, thus breaking the codec's audio output route.

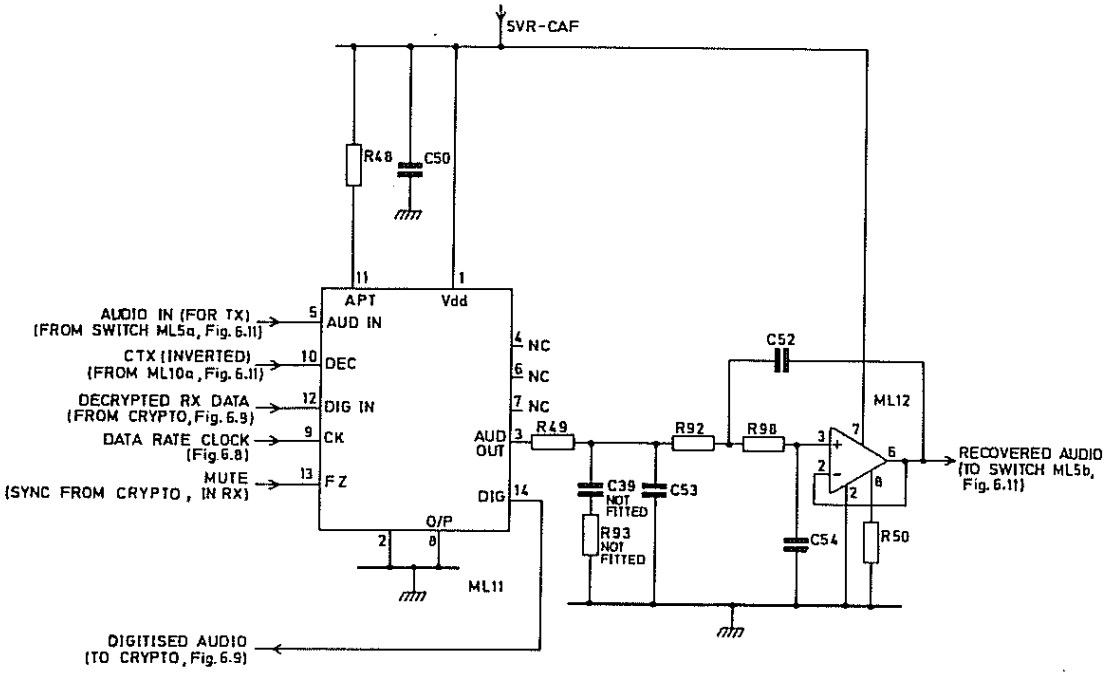


Fig 6.7 Codec

Clock Generator (Fig. 6.8)

24 The clock signals used by the board are produced by the clock generator. Invertor ML6a causes crystal XTL1 to oscillate and ML6b squares-up the 4.096 MHz output, which is divided-down by binary counter ML7. The Q2 (÷4) output from ML7 (pin 7) is Fast Clock (FAC) for the crypto module; the Q4 (÷16) output (pin 15) is the basic 16 x bit rate clock that is adjusted by the clock recovery module to produce the data bit rate clock used by the crypto and codec; the Q5 (÷32) output (pin 3) is used by the transversal filter. The clock circuit is powered by 5VB-CPS (PL1/25). C25 allows adjustment of the oscillator frequency.

Slicer (Fig. 6.8)

25 The slicer, op amp ML13a plus associated components arranged as a comparator, produces a digital representation of RX SIG (PL1/3) as the received data signal goes above and below a mean level set by C28. R55 provides hysteresis, preventing spikes from affecting the output. The output goes via NOR gate ML10d, where it is squared-up and inverted, unless the unit is transmitting, in which case CTX high holds the gate's output low.

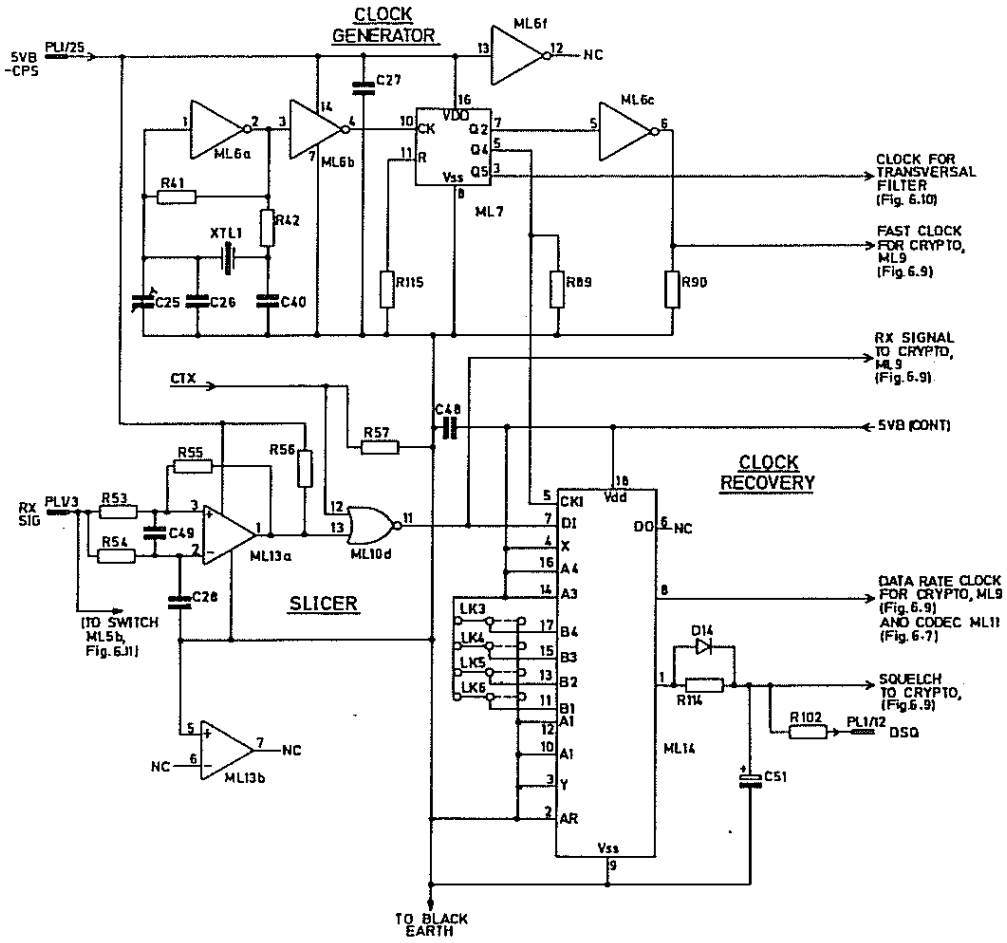


Fig 6.8 Clock Generator, Slicer and Clock Recovery

Clock Recovery (Fig. 6.8)

26 The clock recovery module ML14 divides the 16 x bit rate signal at CKI (pin 15) to data bit rate and adjusts it such that it is in phase with the incoming data at DI (pin 7). The module compares its bit rate clock with the zero crossings of the data and, after 32 early/late decisions have been made, corrects its CKO output (pin 8). If its clock is in advance, it alters its division of the 16 x

bit rate signal: it divides by 17 instead of 16 to retard it. If its clock lags, it divides instead by 15 to speed it up.

27 The module outputs a high SQ (squelch) signal (pin 1) when a valid received signal is present at a level better than a predefined signal/noise ratio. Preset A inputs (pins 10, 12, 14, 16) define the come-in threshold (ie. the S/N ratio at which the circuit decides a signal is present if no signal has been previously detected). Preset B inputs (pins 11, 13, 15, 17) define the go-out threshold (ie. the S/N ratio at which the circuit decides that a signal is no longer usable). The decision is based on counting the proportion of zero crossings that occur at the expected times (ie. at the low-going edges of the recovered clock); for noise, the crossings are randomly distributed.

28 ML14 also divides the 16 x bit rate signal at CKI to provide the CKO bit rate clock used during transmit operations. This avoids discontinuity when the unit switches from receive to transmit and vice versa.

29 The SQ output goes to the crypto module, and leaves the board as DSQ (Digital Squelch) via PL1/12. Diode D14, resistor R114 and capacitor C51 form a fast-rise/slow-fall integrator, so squelch is active for a hang-time of about 1 second after the received signal has ended. This allows for temporary drop-outs in the received signal.

Crypto (and Reversals Control) (Fig. 6.9)

30 The crypto module ML9 performs the encryption and decryption functions. When the unit is switched-on, ML9 is powered partly by the 5VB rail (to pin 1) and partly by 5.6V from the 5V supply isolator. The 5.6V to pin 3 goes via a diode to provide a 5V output 5VR (pin 2). When the unit is switched-off, the 10V BATT supply (PL1/14) powers the parts supplied by 5VR to preserve vital information (eg. keys), and if the battery is removed, capacitor C30 can keep the 5VR-powered parts of the crypto alive for (at least) fifteen minutes.

31 The module outputs a low MAB (Module Absent) signal (pin 12) to indicate its presence on the board. The Fail input (pin 7) is used as an on/off control signal; it is high for on.

32 When XMIT (pin 16) goes high, the crypto module operates in the transmit mode. It carries-out a self test. If the self-test is successful, the module outputs TON (Transmit On) high (pin 13). During the test, and if the test fails (eg. it has no cipher codes), the module outputs a high CRA (Crypto Alarm) signal (pin 24). TON high turns-off FET TR9 and thus energises circuits on the data output route; it also goes to the (off-board) control processor, via PL1/6, to inform it that the crypto is transmitting. CRA high leaves the board via PL1/2 to inform the processor that the crypto is not able to produce a secure transmit output.

33 After a successful self-test the crypto outputs data-rate phase reversals on the TCT (Transmit Cipher Text) line (pin 14) to allow the receiving unit to synchronise its internal clock. While the reversals are being transmitted, they also go, via OR gate ML10c, to counter ML18. When the counter has counted 1024 high-going edges to its clock input (pin 10), its Q10 output (pin 14) goes high. This, inverted to low by ML6e, goes to the crypto's PHE (Phase Enable) input (pin 22), where it terminates the reversals. It also goes to the OR gate (ML10c) where it inhibits further clocking pulses to the counter.

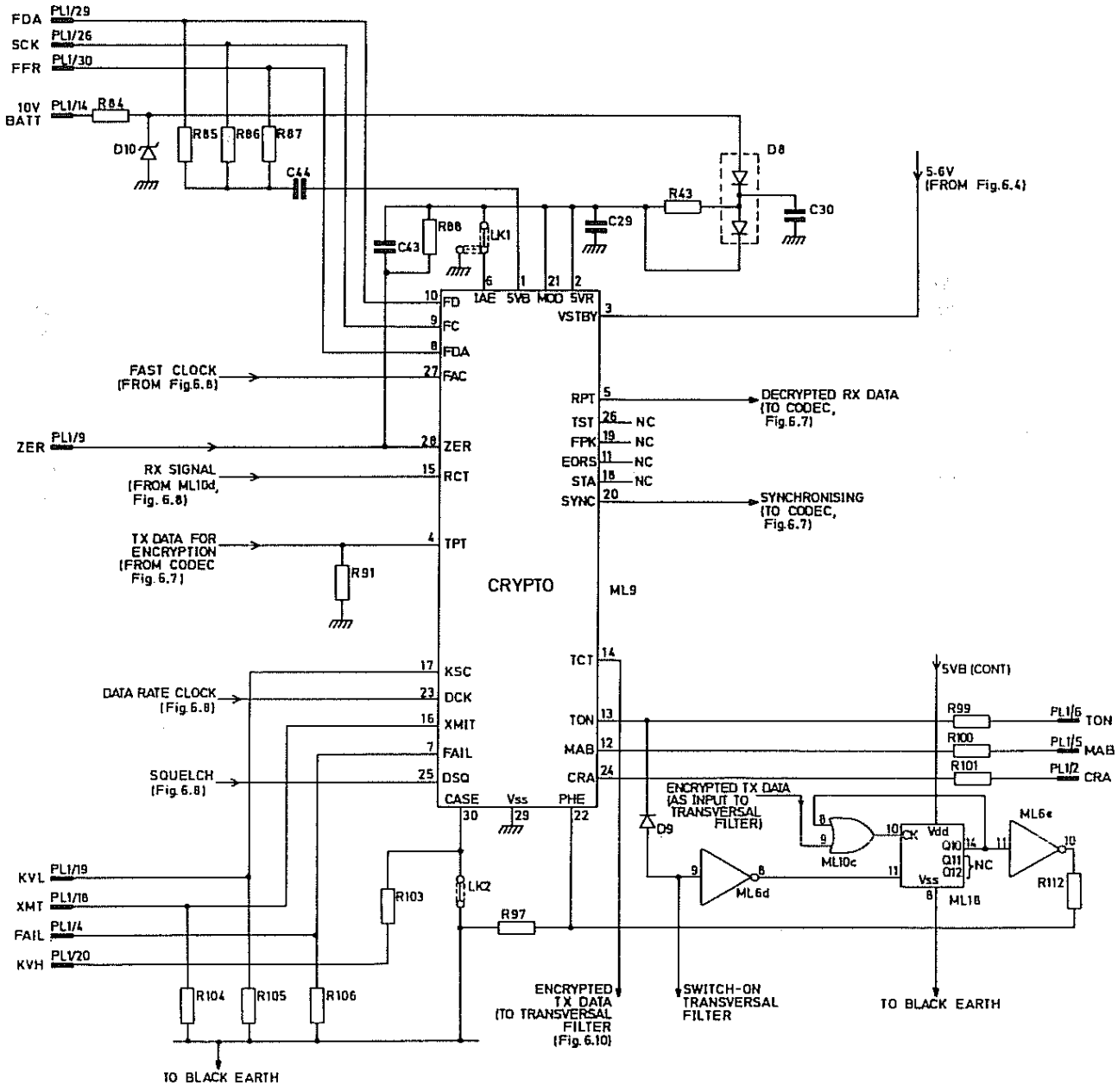


Fig 6.9 Crypto and Reversals Control

34 The crypto generates and sends a sync code. This allows the receiving crypto to set its decryption circuits in the manner required to decrypt the subsequent data. The transmitting crypto also sends updating sync codes at intervals during the transmission. For details see the handbook for the crypto module.

35 After sending the initial sync code, the module encrypts the TPT (Transmit Plain Text) input signal (pin 4) and outputs it as TCT (Transmit Cipher Text, from pin 14). When XMIT goes low, the crypto terminates its encryption operations and makes TON low to inform the processor that it has finished. TON also resets counter ML18 to zero (high signal to pin 11).

36 When DSQ (Data Squelch, pin 25) goes high, the crypto module operates in the receive mode. It first carries-out a self-test, then synchronises its timing and key circuits with the incoming data. During this period it makes Sync (pin 20) low to mute the codec. It then makes Sync high and decrypts the RCT (Received Cipher Text) sliced data (pin 15) and outputs it as RPT (Received Plain Text, pin 5).

37 When the FDA (Fill Data Available) input (pin 8) is high, the cipher code data is clocked into the module via FD (Fill Data, pin 10) by pulses applied to FC (Fill Clock, pin 9). The data bits are valid on both leading and trailing edges of the clock (the data changes while clock is low). KSC (pin 17) selects one of two stored codes for encryption/decryption use. A high input via ZER (Zeroise, pin 28) deletes the stored codes.

38 To prevent current from flowing out from the battery-powered signal sources when the local power rails are off, signals such as RPT (ML9, pin 5) are pulled-up to the local rails via resistors (eg. R44) and diodes (eg. D12) facing the sources of the signals. CMOS signals to/from the board are protected by resistors (eg. R99 on TON).

Transversal Filter (Fig. 6.10)

39 The transversal filter shapes the crypto's encrypted data output to a sinusoidal waveform. The filter consists of eight-bit shift registers ML15, ML16 connected in series. Data is clocked-in via pin 7 of ML15, at 8 x bit rate, and the parallel outputs from the registers are connected together via resistors.

40 When the input data is high, the register fills with high bits. If the next data bit is high, the register remains full of high bits, so its outputs are all high. If the next data bit is low, the register fills up with low bits and the outputs go low, one at a time, until all are low. The resulting output from the connected parallel outputs is a current with a value that, at any time, depends on the number of high bits in the register. The choice of resistor values causes a rounded-off (sinusoidal) representation of the original squarewave, and this is more suitable for transmission.

41 The output from the shift registers goes to op amp ML17 which (with associated components) further rounds-off the waveform. It provides a raised cosine version of the data, with the level set by R77, R78. The signal goes via ML8b, switched through by SEC low, and onto the TX SIG line (PL1/28).

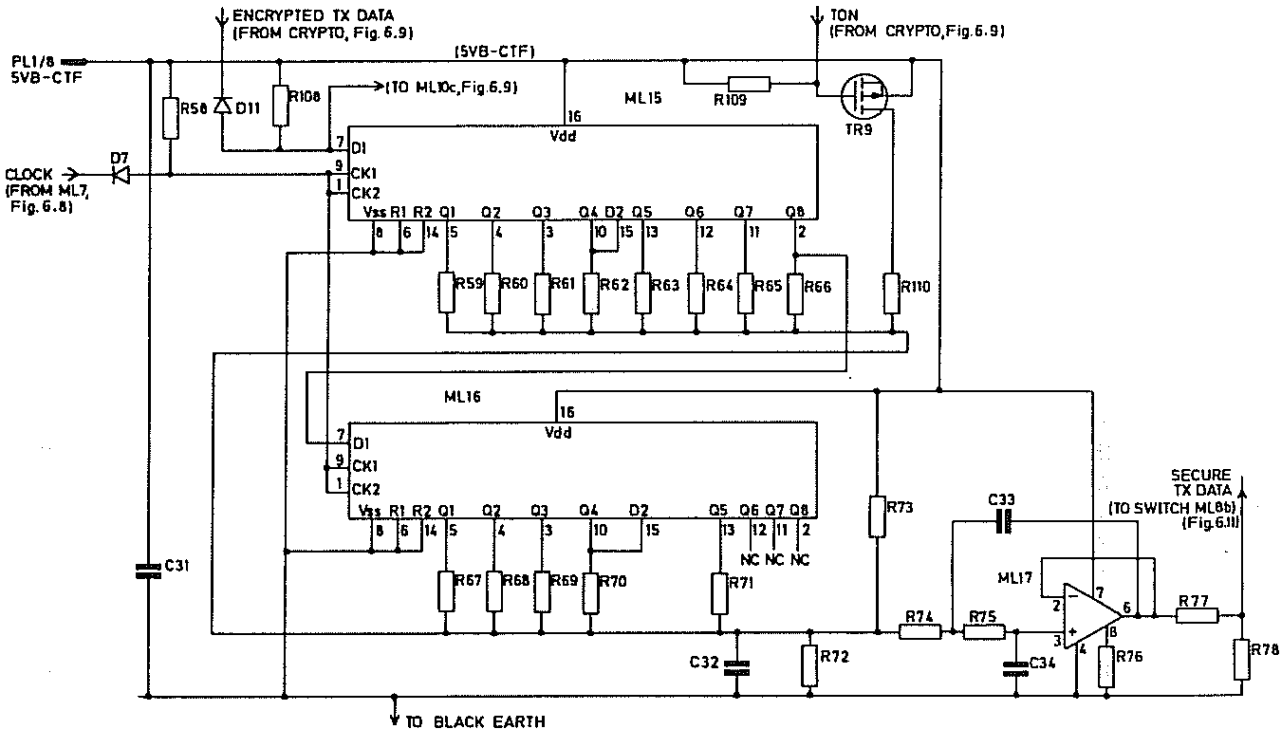


Fig 6.10 Transversal Filter

42 FET TR9 provides bias control. It produces a mid-range input to op amp ML17 from the start of transmission (5VB-CTF high) until data starts to arrive from the shift registers (TON high), and thus prevents a large swing on the output line at the start of the data output operation.

43 The clear/secure switch ML5c, ML8c, ML8b is in three parts to ensure high isolation between the unselected clear input to ML5c and the selected secure output from ML8b, so leakage of clear signals into the secure transmission is minimised.

FUNCTIONAL TESTS AND ALIGNMENT

44 Functional tests and alignment procedures for the Crypto Board are detailed in Tables 2 to 7. There is very little alignment: adjustments can be made only in the two tests shown in Table 2. The other tests check correct working of various parts of the circuit and can therefore be used to identify the source of a fault, and to confirm correct operation after a repair.

45 For the tests, operate the Crypto Board with the remaining parts of a known-working PRM4515U. To allow access to all parts of the board, connect the Crypto Board to the Control Board via Extender Cable TJ2085. Apply a 10 V ± 0.1 V supply to the battery terminals of the PRM4515U, using Battery Adaptor TJ2017 (ensure correct polarity).

46 Set the unit to Clear mode and Channel 0, with the OFF/Volume switch at position 1 (first ON position), unless otherwise instructed in the procedures. Measure Transmit signals with 1 kHz at 5 mV p-p into Pin A, Normal Sensitivity. Apply a similar signal (but 2 mV p-p) at the 'test transmitter' for receive tests. The voltages shown in the tables are with respect to chassis 0 V, and pins are open-circuit unless specified. For Secure mode tests, a crypto module, filled with suitable cipher codes, must be fitted to the board, and the 'test transmitter' radio must have the same codes.

TYPICAL VOLTAGES AND WAVEFORMS

47 Typical voltages and waveforms are shown in Table 8. The board under test is set-up as for the functional tests (Para. 45), with access available to all parts and power connected. No other external inputs are used for the static tests.

48 Set the unit to Channel 0 and noise-on (OFF/Volume switch set to position 7).

49 If a crypto module is not fitted on the board, the Secure mode tests are not necessary.

EQUIPMENT REQUIRED FOR BOARD TESTS

(1) DC Power Supply

Range	:	0 V to 30 V
Current	:	1 A
Example	:	Farnell L30-2

(2) Oscilloscope

Range	:	20 MHz adequate
Impedance	:	1 MΩ
Example	:	Hewlett Packard 1740B

(3) Digital Multimeter

Range	:	0 V to 5 V
Current	:	0 to 10 mA
Example	:	Solartron 7050

(4) Frequency Counter

Range	:	0 Hz to 10 MHz
Resolution	:	0.1 Hz
Example	:	Racal 9009

(5) AF Signal Generator

Range	:	0 Hz to 10 kHz
Output Voltage	:	0 V to 5 V rms
Example	:	Advance J3B
		Note: Balanced output required

(6) Millivoltmeter

Range	:	0.1 mV to 10 V
Example	:	Bruel & Kjaer 2425

(7) Test Aids

Extender Cable, 32-way, TJ2085
Audio Interface Jig BCC TJ1117
Battery Adaptor, TJ2017

(8) Ancillaries

Known-working PRM4515U for use as 'test transmitter'.

TABLE 1

Interboard Connector Listing

Pin	I/O	Signal
PL2 (To/from Control Board)		
1	O	FLA. Fixed-level audio select.
2	O	CRA. Crypto alarm.
3	I	RAD. Received signal (demodulated).
4	I	Fail.
5	O	MAB. Crypto module absent.
6	O	TON. Crypto transmitting.
7	O	RXAUD. Received signal processed by Crypto Board
8	I	CTF. Transversal filter power control.
9	I	ZER. Zeroise (erase codes).
10		0 V.
11	I	8VB.
12	O	DSQ. Digital squelch.
13	I	CTX. Transmit control.
14	I	10 V Batt.
15	I	Pin A. Mic/data/FLA program signal.
16	I	5VB.
17	I	SEC. Secure select.
18	I	XMT. Transmit control.
19	I	KVL
20	I	KVH Cipher code select (KVH not used)
21	I	CAF. Audio filter power control.
22	I	WIE. Wideband select.
23		-
24		0 V.
25	I	CPS. Crypto clock generator power control. Held high.
26	I	SCK. Clock for crypto fill.
27		-
28	O	TX SIG. Signal for transmission.
29	I	FDA. Crypto fill data.
30	I	FFR. Crypto fill frame.
31	O	WB AUD. Received wideband signal.
32	I	WHI. Whisper select.

TABLE 2

Power Rail Tests

Supply	Pin	Mode	Voltage	Current (Approx)
8vB	PL1/11	Tx	8 V	6 mA
5VB	PL1/16	-	5 V	
10 V Batt	PL1/14	-	10 V	170 µA
5VB-CPS	PL1/25	Tx	5 V	2 mA
5VB-CTF	TL1/8	Tx	5 V	600 µA

TABLE 3

Alignment

Test	Radio Mode	Inputs	Monitor	Limits	Notes
Crystal Oscillator Frequency	Clear, Rx		ML9/27	Squarewave 1024000±1Hz	Adjust C25
Vogad Output Level	Clear, Rx	1kHz Sinewave 2mV rms at Pin A (of Audio socket)	ML4/7	0.37±0.05V rms	Adjust R29

TABLE 4

Clear Transmit Tests

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
1	5.6 supply	Clear, Tx		ML9/3	5.6±0.25V	
2	Vogad gain (Normal)	Clear, Tx Vol Sw posn 4	800 Hz,1mV rms at Pin A (Audio socket)	TP1	0.35±0.1V	
3	Vogad gain (Whisper)	Clear Tx Vol Sw posn 1	800Hz,0.25mV rms at Pin A	TP1	0.35±0.1V	
4	Vogad gain (FLA)	Clear, Tx Vol Sw posn 4	800Hz,10mV rms, and 1ma into Pin A	TP1	0.35±0.1	
5	Wideband (WB)	WB, Tx	1mA into Pin B. 800Hz,0.46V rms at Pin A	PL1/28	0.46±0.1V	
6.1	Audio filter response	Clear, Tx	1kHz sinewave, 2mV at Pin A	PL1/28	0.37±0.1V	
6.2			As Test 6.1 but 150Hz		-30dB	Minimum attenuation compared with result of Test 6.1
6.3			As 6.1 but 310Hz		-60dB	
6.4			As 6.1 but 3300Hz		-6dB	

TABLE 5

Secure Transmit Tests (Crypto Module ML9 Fitted)

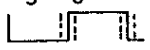
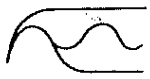
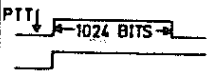
Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
1	Back-up capacitor	Secure, Tx		Cathode of D10	5.6±0.3V	Wait for C30 to fully charge before taking measurement.
2	Xtal oscillator			ML9/27	1.024MHz ±1Hz	
3	Codec modulation	Secure, Tx	1kHz sinewave 2.0mV rms	ML9/4	Fully-modulated 1kHz	1kHz square-wave with 10% edge jitter 
4	Encrypted data	Sec, Tx		ML9/14	0/5V data	Continuous stream of random data
5	Transveral filter	Sec, Tx		PL1/28	60% 'Eye' pattern	
6	Phasing counter	Sec, Tx	PTT	ML9/22 ML9/13	+ve Pulse for 1024 TCT bits	

TABLE 6

Clear Receive Tests

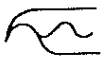
Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
1	Receive signal	Clear, Receive	100µV, 5kHz deviation RF signal from test transmitter (or signal generator). Use 1kHz, 2mV sinewave audio input to 'test transmitter'.	PL1/7	0.40±0.1V	

TABLE 7

Secure Receive Tests

Test No.	Test	Radio Mode	Inputs	Monitor	Limits	Notes
1	Slicer	Sec, Rx	Secure RF signal (from 4515 'test transmitter')	ML9/15	0V/5V square wave	Ensure transmit and receive crypto codes are the same
2	Clock recovery	Sec, Rx	As Test 1	ML9/23 ML9/15	Correct phase relation-ship between recovered clock and I/P signal	Trigger scope on pin ML9/15. Check ML9/23 is locked in sync with ML9/15, and ML9/23 neg edges coincide with changes of state of ML9/15
3	Digital squelch on	Sec, Rx	As Test 1	PL1/12	H	H = 5±0.2V
4	Crypto Sync	Sec, Rx	As Test 1	ML9/20	H	Audio signal until crypto sync acquired
5	Demodulated data	Sec, Rx	As Test 1	PL1/31	0.5±0.2V	
6	Digital squelch off	Standby	Test signal off	PL1/12	L (after approx 1 sec delay)	L = 0V±0.2V

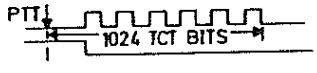
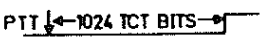
TABLE 8
Static Reference Voltages
(No External Inputs)

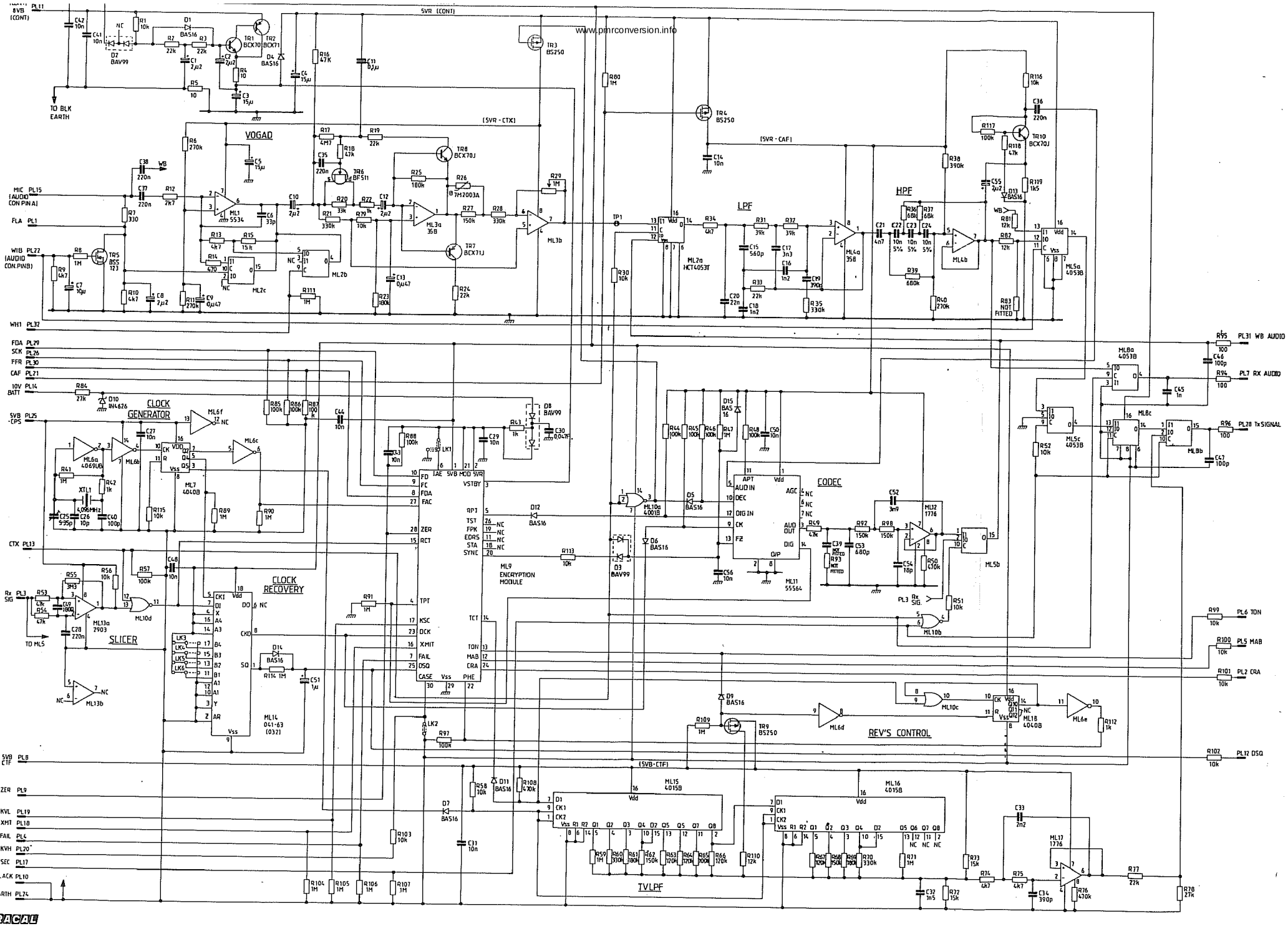
	Clear, Rx,		Clear, Tx		Sec, Rx		Sec, Tx		AC Waveforms and Notes
	DC	AC	DC	AC	DC	AC	DC	AC	
TR1	e 5.9		-		-		-		Where - is shown instead
	b 6.2		-		-		-		of a number, there is no
	c 7.4		-		-		-		change from Clear, Rx, Noise-On.
TR2	e 8.0		-		-		-		AC voltages are shown
	b 7.4		-		-		-		only when a significant
	c 5.9		-		-		-		signal is present.
TR3	s 5		5		-		-		L = 0V ± 0.2V
	g H		L		-		-		H = 5 ± 0.2V
	o 0		5		-		-		
TR4	s 5		5		-		-		
	g H		L		-		-		
	d 0		5		-		-		
TR5	s 0		-		-		-		
	g 0		-		-		-		5V when WB selected
	d 0		-		-		-		5V when FLA selected
TR6	s		4.6				-		
	g		3.0				-		
	d		4.6				-		
TR7	e		1.6	1p-p			-		Sinewave
	b		1.6				-		
	c		0.1				-		
TR8	e		1.6	1p-p			-		Sinewave
	b		1.6				-		
	c		3.0				-		
TR9	s						5.2		
	g						4.7		0 during initial 10ms after PTT
	d						2.6	2p-p	'Eye' waveform: 
TR10	e 0.5	1p-p							
	b 1.0	1p-p							
	c 2.3	3p-p							

ML	Pin	Clear, Rx,		Clear, Tx		Sec, Rx		Sec, Tx		AC Waveforms and Notes
		DC	AC	DC	AC	DC	AC	DC	AC	
1	1			NC						NC = not connected
	2			2.5						
	3			2.5						
	4			0						
	5			NC						
	6			2.5	10mV p-p					Sinewave
	7			4.9						
	8			NC						
2	1	0		2.5						
	2	NC								
	3	NC								
	4	0		2.5						
	5	0		2.5						
	6	0								
	7	0								
	8	0								
	9	L								H when Whisper selected (Vol Sw posn 1 or 2).
	10	0								H when FLA selected
	11	L		H						
	12	2		0.5						
	13	0		1.8	1.3-pp					Sinewave
	14	2		1.8	1.3-pp					Sinewave
	15	0		2.5						
	16	5.5		4.9						
3	1			1.6	1.0-pp					Sinewave
	2			1.6						
	3			1.6						
	4			0						
	5			1.7						
	6			1.7						
	7			1.8	1.3-pp					Sinewave
	8			4.9						
4	1	1.9	2p-p	1.8	1p-p					Sinewave
	2	1.9	2p-p	1.8	1p-p					Sinewave
	3	1.9	2p-p	1.8	1p-p					Sinewave
	4	0								
	5	2.0	2p-p		1p-p					Sinewave
	6	2.0	2p-p		1p-p					Sinewave
	7	2.0	2p-p		1p-p					Sinewave
	8	5.0								

ML	Pin	Clear, Rx,		Clear, Tx		Sec, Rx		Sec, Tx		AC Waveforms and Notes
		DC	AC	DC	AC	DC	AC	DC	AC	
	11	NC								
	12	0								
	13	L		L		L		H		
	14	0		0		0			5p-p	16kb/s data, squarewave
	15		5p-p							
	16	L		L		L		H		
	17	L								H when Sec B selected
	18	NC								
	19	NC								
	20	L		L		H		L		
	21	H								PTT
	22	L		L		L		As Fig		1024 TCT BITS
	23		5p-p							Squarewave, 16kHz
	24	L								
	25	L		L		H		L		
	26	NC								
	27		5p-p							Squarewave, 1MHz
	28	H								L when zeroise is selected
	29	0								
	30	0								
10	1	L		H		L		H		
	2	L		H		L		H		
	3	H		L		H		L		
	4	L		L		H		L		
	5	L		H		L		H		
	6	H		H		L		L		
	7	0								
	8	L		L		L		H		
	9	0		0		0			5pp	16kb/s data, squarewave
	10	H		H		H			5pp	PTT 1024 TCT BITS
	11		5p-p	L			5p-p	L		
	12	L		H		L		H		
	13		5p-p	H			5p-p	H		
	14	5								
11	1	5								
	2	0								
	3	2.6	-	2.5	1p-p	2.6	1p-p	2.5	1p-p	
	4	NC								
	5	2.5	4p-p	2.5	3p-p	2.5	3p-p	2.5	3p-p	Sinewave
	6	NC								
	7	NC								
	8	0								

ML	Pin	Clear, Rx,		Clear, Tx		Sec, Rx		Sec, Tx		AC Waveforms and Notes
		DC	AC	DC	AC	DC	AC	DC	AC	
	9		0.5to 4.5							Squarewave, 16kHz
	10	4.5		0.5		4.5		0.5		
	11	H								
	12	0.5		0.5		0.5to 4.5		0.5to 4.5		16kb/s data, squarewave
	13	0.5		4.5		4.5		4.5		
	14	I	5p-p	5	5p-p	5	5p-p	5	5p-p	I = Idle pattern (16kb/s squarewave) S = modulated Signal
12	1	NC								
	2	2.7		2.7	1.5p-p	2.7	1.5p-p	2.7	1.5p-p	Sawtooth (symetrical)
	3	2.7		2.7	1.5p-p	2.7	1.5p-p	2.7	1.5p-p	Sawtooth (symetrical)
	4	0								
	5	NC								
	6	2.7		2.7	1.5p-p	2.7	1.5p-p	2.7	1.5p-p	Sawtooth (symetrical)
	7	5								
	8	4.5								
13	1		5p-p	5		5p-p		5		
	2	~ 2*		0.4		2*		0.4		* mean of Rx signal
	3		1.5p-p	0.6			1.5p-p	0.6		
	4	0								
	5	NC								
	6	NC								
	7	NC								
	8	5								
14	1	L		L		H		L		
	2	0								
	3	0								
	4	5								
	5		5p-p							Squarewave, 256 kHz
	6	NC								
	7		5p-p				5p-p	H		
	8		5p-p							Squarewave, 16 kHz
	9	0								
	10	0								
	11	5								
	12	0								
	13	5								
	14	5								
	15	5								
	16	5								
	17	5								
	18	5								

ML	Pin	Clear, Rx,		Clear, Tx		Sec, Rx		Sec, Tx		AC Waveforms and Notes
		DC	AC	DC	AC	DC	AC	DC	AC	
15	1	L		L		L			5p-p	Squarewave, 128 kHz
(&	2	L		L		L			5p-p	Data, 16kb/s, squarewave
ML	3	L		L		L			5p-p	Data, 16kb/s, squarewave
16)	4	L		L		L			5p-p	Data, 16kb/s, squarewave
	5	L		L		L			5p-p	Data, 16kb/s, squarewave
	6	0								
	7	L		L		L			5p-p	
	8	0								
	9	L		L		L			5p-p	Squarewave, 128 kHz
	10	L		L		L			5p-p	Data, 16kb/s, squarewave
	11	L		L		L			5p-p	Data, 16kb/s, squarewave
	12	L		L		L			5p-p	Data, 16kb/s, squarewave
	13	L		L		L			5p-p	Data, 16kb/s, squarewave
	14	0								
	15	L		L		L			5p-p	Data, 16kb/s, squarewave
	16	5								
17	1	NC								
	2	L		L		L			2p-p	'Eye' (as TR9d)
	3	L		L		L			2p-p	'Eye' (as TR9d)
	4	0								
	5	NC								
	6	L		L		L			2p-p	'Eye' (as TR9d)
	7	5								
	8	4.5								
18	1	NC								
	2	NC								
	3	NC								
	4	NC								
	5	NC								
	6	NC								
	7	NC								
	8	0								
	9	NC								
	10	H		H		H			5p-p	
	11	H		H		H		As Fig		
	12	NC								
	13	NC								
	14	L						As Fig		
	15	NC								
	16	5								

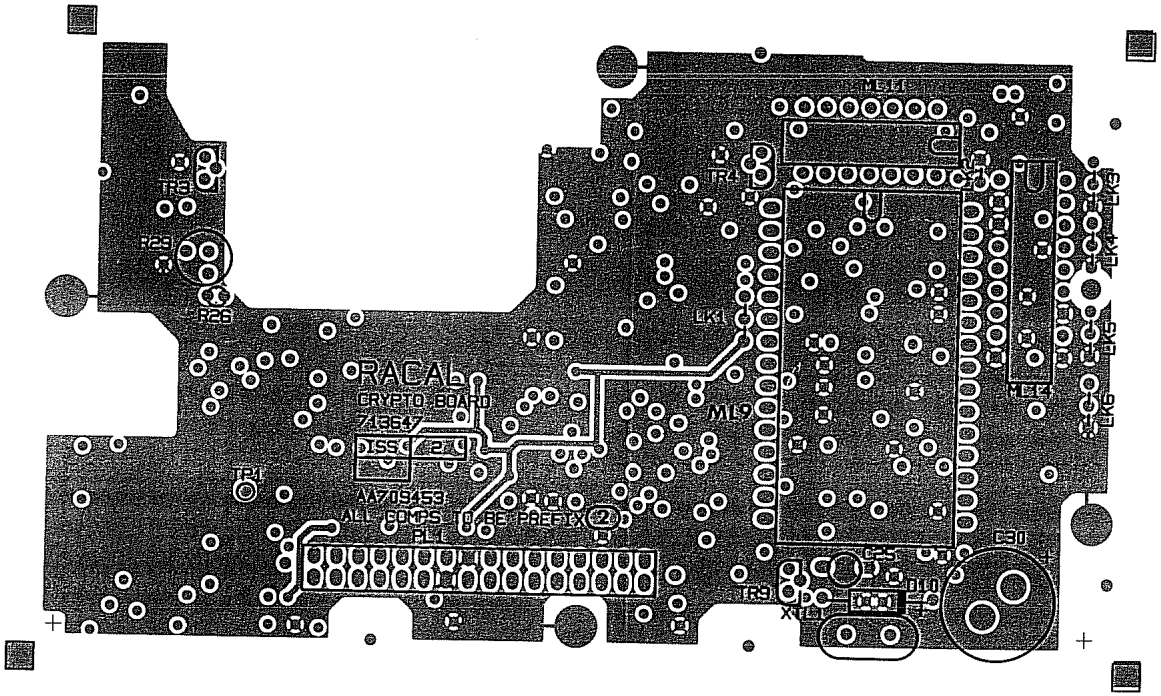


RACAL

TH 7158	EC 709453
3	

Circuit: Crypto Board

Fig.6.11



RACAL

TH7158	713647
2	

Crypto Board : Layout
(Sheet 2)

Fig. 6.12

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CHAPTER 7

INTERCONNECTIONS, SWITCH AND DECOUPLING BOARDS

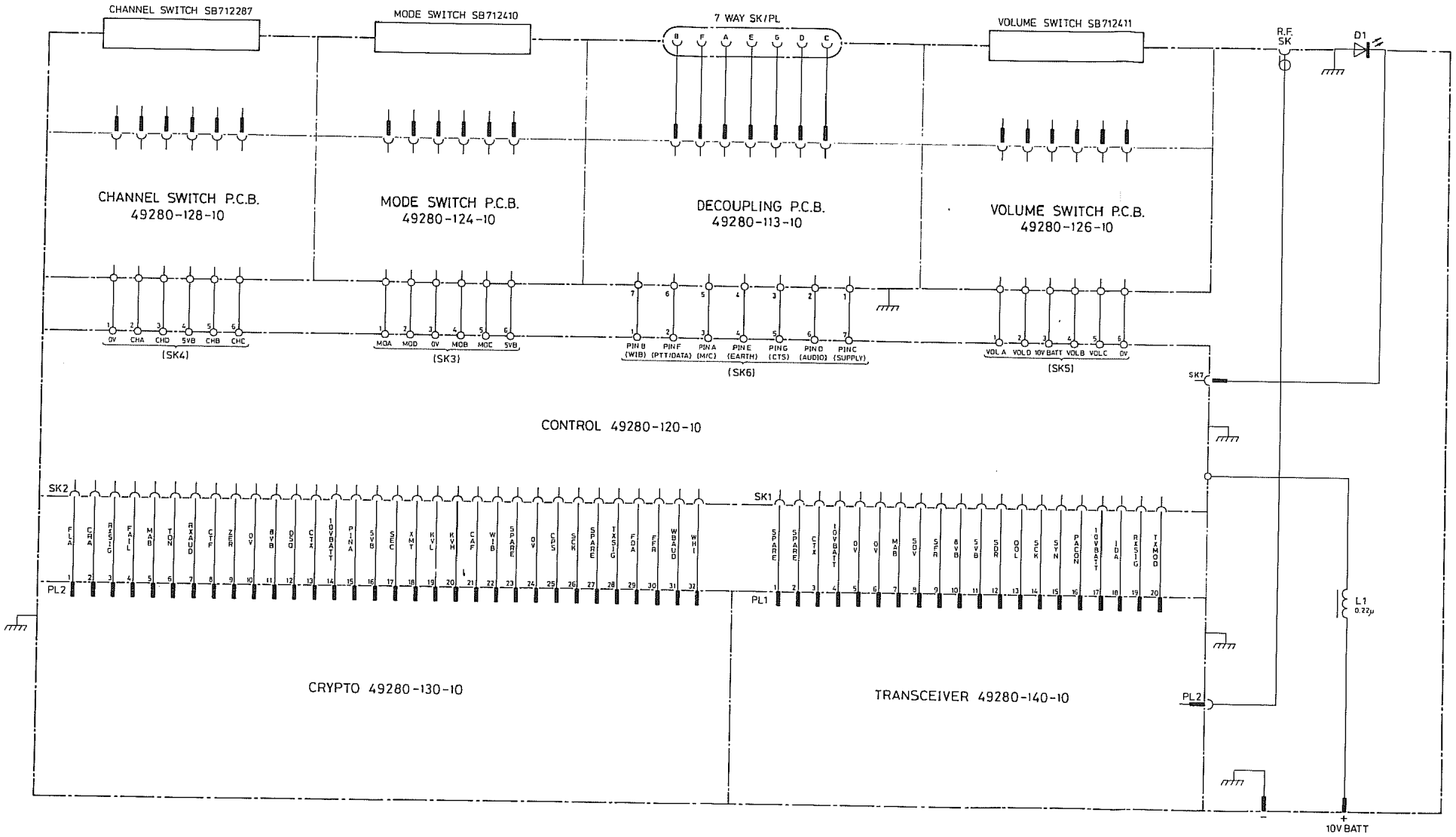
CONTENTS

	Page
INTERCONNECTIONS	7-1
SWITCH AND DECOUPLING BOARDS	7-1

ILLUSTRATIONS

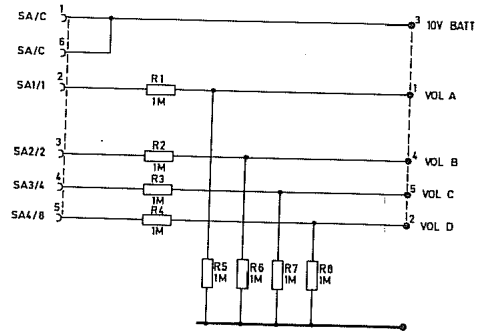
Fig. No.

7.1	PRM4515U: Interconnections
7.2	Small PCBs: Circuits
7.3	Small PCBs: Layouts



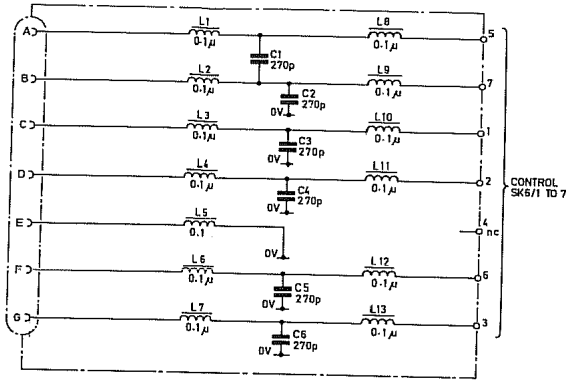
RACAL
TH7158 | 79280-102-10
A

PRM4515U : Interconnections Fig. 7.1



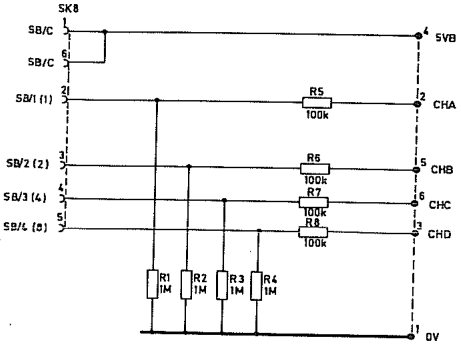
VOLUME SWITCH BOARD

BC709448 Issue 1



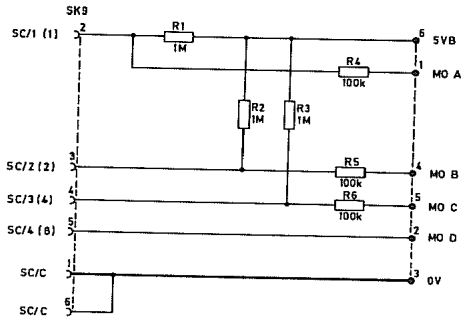
DECOUPLING (AUDIO) BOARD

79280-114-10 Issue B



CHANNEL SWITCH BOARD

BC709450 Issue 1



MODE SWITCH BOARD

BC709449 Issue 1

RACAL
TH7150

Small PCBs : Circuits

Fig. 7.2

CHAPTER 8

DISMANTLING, FAULT LOCATION AND ALIGNMENT

CONTENTS

	Page
DISMANTLING AND ASSEMBLING THE PRM4515U	8-1
Access to Inside the Unit	8-1
Removing the Crypto Board	8-1
Removing the Transceiver Board	8-2
Removing the Control Board Assembly	8-2
FAULT LOCATION AND ALIGNMENT	8-3
PRESSURE TEST	
APPENDIX 1: MAINTENANCE OF UNITS EMPLOYING SURFACE MOUNTED COMPONENTS	

CHAPTER 8

DISMANTLING, FAULT LOCATION AND ALIGNMENT

DISMANTLING AND ASSEMBLING THE PRM4515U (Figs. 1.2, 1.3)

1 Dismantling instructions are given in the following paragraphs; to reassemble the unit, reverse the dismantling sequence unless otherwise stated. Disconnect all cables and power before dismantling the unit. Dismantle only in a clean dry environment and on a suitable surface. If the desiccator sachet is pink or purple, replace it with a fresh blue one, and, to check that the unit is sealed correctly, carry-out a pressure test before returning it to service.

Access to Inside the Unit

2 With all power and cables disconnected, slacken the 18 (9 each side) captive screws that secure the side covers. When refitting the side covers, check that the seals (fixed to the covers) are undamaged.

Removing the Crypto Board

3 Remove the four slot-head M2.5 screws that secure the Crypto Board to the pillars that separate it from the centrally-mounted Control Board. The screws have crinkle washers.

4 Carefully pull the Crypto Board away from the Control Board to disengage the plug/socket connection between the two boards (PL1/SK2 in Fig. 1.3).

5 The crypto module is a plug-in item on the Crypto Board (Fig. 1.3).

APPENDIX 1

MAINTENANCE OF UNITS EMPLOYING SURFACE MOUNTED DEVICES (SMDs)

1 The use of surface mounted devices in industry is increasing at a rapid rate. It is conceivable that within a few years the use of SMDs will predominate over the "conventional leaded components" currently in use. The reasons for this include the ease of automated manufacturing techniques, thus moving away from an expensive labour-intensive assembly line and incurring no extra costs.

2 The reduced size of the SMDs allows either:

(a) the completed unit to be reduced in size, or

(b) for a given size, more facilities to be incorporated into the unit or PCB.

3 Initially, it may appear from the increased component density that boards comprising SMDs will be more difficult to work with than those comprising the more conventional leaded components.

4 It will be found that, by using the standard diagrams, component layouts, etc., contained in the technical manual, fault finding and component identification is comparable with existing procedures and techniques.

5 Removal of SMDs may be accomplished with a standard 25W temperature controlled soldering iron and suitable tweezers, provided care is taken to avoid closely-mounted neighbouring components.

6 Replacement devices may be fitted to the PCB with the same ease of operation, again using a standard 25W temperature controlled soldering iron and suitable tweezers. It will be found that the lack of plated through holes makes component removal/replacement less likely to lead to secondary damage to the PCB, i.e. the risk of damage to tracks, pads and adjacent components is greatly reduced.

CHAPTER 9

COMPONENTS LIST

CONTENTS

	Page
MAIN ASSEMBLY (49280-100-10)	9-1
TRANSCEIVER BOARD ASSEMBLY 4 (49280-140-10)	9-1
CONTROL BOARD ASSEMBLY 2 (49280-118-10)	9-11
CONTROL BOARD A (49280-120-10)	9-11
CRYPTO BOARD ASSEMBLY A (49280-130-10)	9-17
VOLUME SWITCH BOARD ASSEMBLY (49280-126-10)	9-23
DECOUPLING BOARD ASSEMBLY (49280-113-10)	9-23
CHANNEL SWITCH BOARD ASSEMBLY (49280-128-10)	9-24
MODE SWITCH BOARD ASSEMBLY (49280-124-10)	9-24

ILLUSTRATIONS

Fig. No.

9.1 PRM4515U: Exploded View

CHAPTER 9

COMPONENTS LIST

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
		MAIN ASSEMBLY (49280-100-10)			
Items on the main assembly are shown in Fig 9.1.					
		TRANSCEIVER BOARD ASSEMBLY 4 (49280-140-10)			
Resistors (ohms)			W		
R1	22k	Chip	0.0625	±5	28181-305-01
R2	200k	Variable		±10	28361-022-00
R3	68k	Chip	0.0625	±5	28181-317-01
R4	47k	Chip	0.0625	±5	28181-313-01
R5	100k	Chip	0.0625	±5	28181-321-01
R6	4k7	Chip	0.0625	±5	28181-289-01
R7	10k	Variable		±10	28361-016-00
R8	1k8	Chip	0.0625	±5	28181-279-01
R9	47k	Chip	0.0625	±5	28181-313-01
R10	150	Chip	0.0625	±5	28181-253-01
R11	20k	Variable		±20	28361-317-08
R12	150	Chip	0.0625	±5	28181-253-01
R13	47	Chip	0.0625	±5	28181-241-01
R14	100k	Variable		±10	28361-021-00
R15	10	Chip	0.0625	±5	28181-225-01
R16	220k	Chip	0.0625	±5	28181-329-01
R17	56k	Chip	0.0625	±5	28181-315-01
R18	10k	Chip	0.0625	±5	28181-297-01
R19	22k	Chip	0.0625	±5	28181-305-01
R20	5k6	Chip	0.0625	±5	28181-291-01
R21	10	Chip	0.0625	±5	28181-225-01
R22	1k8	Chip	0.0625	±5	28181-279-01
R23	10k	Chip	0.0625	±5	28181-297-01
R24	330	Chip	0.0625	±5	28181-261-01
R25	220	Chip	0.0625	±5	28181-257-01

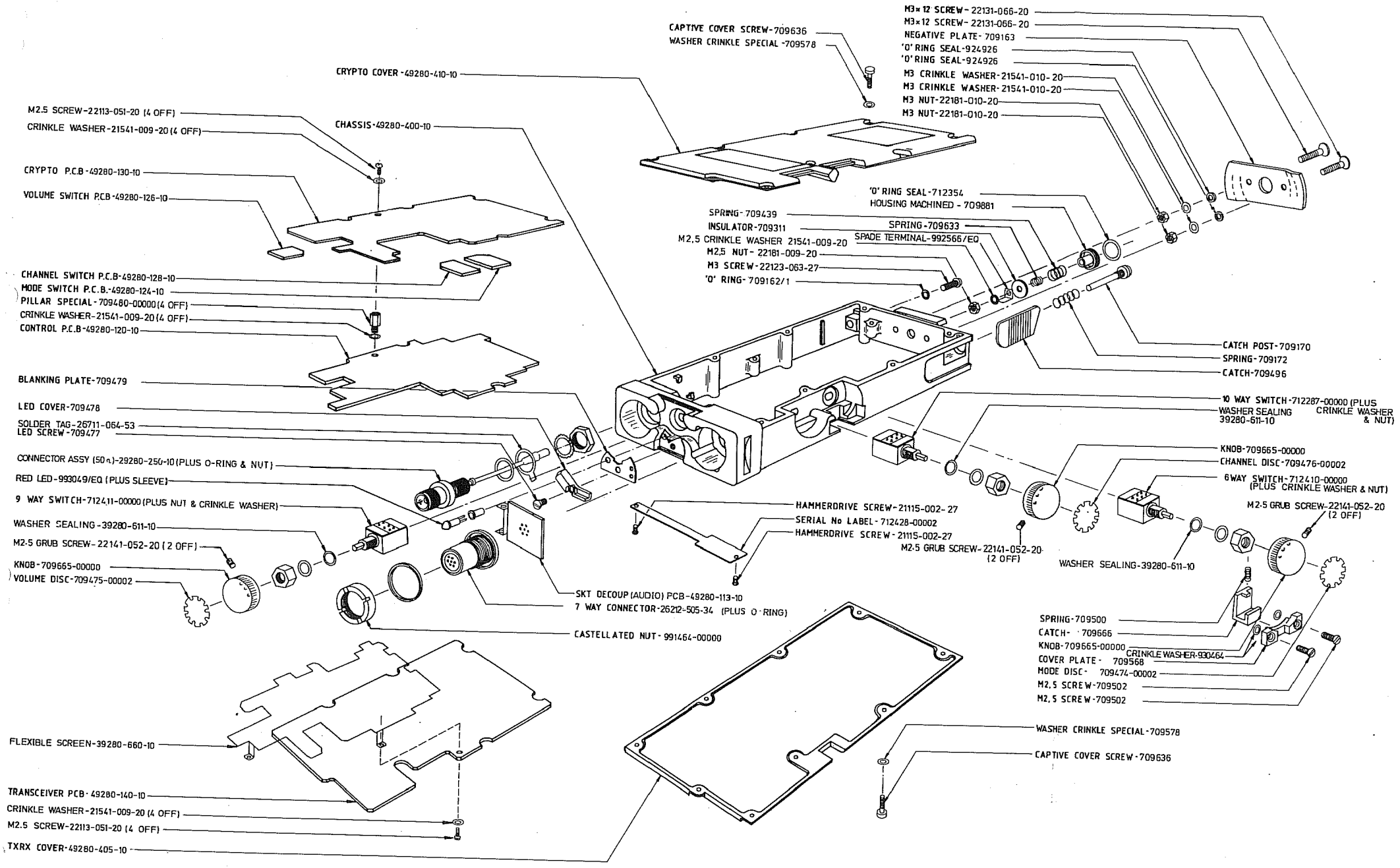
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R26	22k	Chip	0.0625	±5	28181-305-01
R27	56k	Chip	0.0625	±5	28181-315-01
R28	33k	Chip	0.0625	±5	28181-309-01
R29	3k3	Chip	0.0625	±5	28181-285-01
R30	3k3	Chip	0.0625	±5	28181-285-01
R31	1M	Chip	0.0625	±5	28181-345-01
R32	1k5	Metal Oxide	0.125	±5	28141-077-01
R33	39k	Chip	0.0625	±5	28181-311-01
R34	1k	Chip	0.0625	±5	28181-273-01
R35	270	Chip	0.0625	±2	28181-259-02
R36	8k2	Chip	0.0625	±5	28181-295-01
R37	2k7	Metal Oxide	0.125	±5	28141-093-01
R38	8k2	Chip	0.0625	±5	28181-295-01
R39	100	Chip	0.0625	±5	28181-249-01
R40	100	Chip	0.0625	±5	28181-249-01
R41	1k5	Chip	0.0625	±5	28181-277-01
R42	6k8	Chip	0.0625	±5	28181-293-01
R43	39	Chip	0.0625	±5	28181-239-01
R44	12	Metal Oxide	0.125	±2	28141-027-02
R45	Not used				
R46	10k	Metal Oxide	0.25	±5	28141-297-01
R47	10k	Metal Oxide	0.125	±5	28141-097-01
R48	220	Chip	0.0625	±5	28181-257-01
R49	220	Chip	0.0625	±5	28181-257-01
R50	1k8	Chip	0.0625	±5	28181-279-01
R51	470	Chip	0.0625	±5	28181-265-01
R52	120	Chip	0.0625	±5	28181-251-02
R53	22k	Chip	0.0625	±5	28181-305-01
R54	10k	Chip	0.0625	±5	28181-297-01
R55	1k	Chip	0.0625	±5	28181-273-01
R56	10k	Chip	0.0625	±5	28181-297-01
R57	15	Chip	0.0625	±5	28181-229-01
R58	4.7	Metal Oxide	0.25	±5	28141-217-01
R59	470	Metal Oxide	0.125	±5	28141-065-01
R60	120	Metal Oxide	0.125	±5	28141-051-01
R61	1k	Chip	0.0625	±5	28181-273-01
R62	22	Chip	0.0625	±5	28181-233-01
R63	47	Chip	0.0625	±5	28181-241-01
R64	6k8	Chip	0.0625	±5	28181-293-01
R65	2k7	Chip	0.0625	±5	28181-283-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R66	15k	Chip	0.0625	±5	28181-301-01
R67	10k	Metal Oxide	0.125	±2	28141-097-02
R68	100	Variable		±10	28361-006-00
R69	4.7	Metal Oxide	0.25	±5	28141-217-01
R70	150k	Chip	0.0625	±5	28181-325-01
R71	6k8	Chip	0.0625	±5	28181-293-01
R72	2k2	Chip	0.0625	±5	28181-281-01
R73	1k	Chip	0.0625	±5	28181-273-01
R74	22k	Chip	0.0625	±5	28181-305-01
R75	22k	Chip	0.0625	±5	28181-305-01
R76	22k	Metal Oxide	0.25	±2	28141-305-02
R77	180	Metal Oxide	0.25	±5	28141-255-01
R78	2k2	Chip	0.0625	±5	28181-281-01
R79	Not used				
R80	12k	Chip	0.0625	±5	28181-299-01
R81	-	Thermistor, 120°C, 40V			28251-923-00
R82	12k	Chip	0.0625	±5	28181-299-01
R83	1	Metal Oxide	0.25	±5	28141-201-01
R84	68k	Chip	0.0625	±5	28181-317-01
R85	22k	Chip	0.0625	±5	28181-305-01
R86	180	Metal Oxide	0.125	±5	28141-055-01
R87	1	Metal Oxide	0.25	±5	28141-201-01
R88	100k	Metal Oxide	0.25	±5	28141-321-01
R89	10k	Metal Oxide	0.125	±2	28141-097-02
R90	15k	Chip	0.0625	±5	28181-301-01
R91	1k	Chip	0.0625	±5	28181-273-01
R92	33k	Metal Oxide	0.125	±5	28141-109-01
R93	6k8	Metal Oxide	0.125	±2	28141-093-02
R94	1M	Chip	0.0625	±5	28181-345-01
R95	820	Metal Oxide	0.125	±5	28141-071-01
R96	1M	Chip	0.0625	±5	28181-345-01
R97	1M	Chip	0.0625	±5	28181-345-01
R98	1M	Chip	0.0625	±5	28181-345-01
R99	1M	Chip	0.0625	±5	28181-345-01
R100	1M	Chip	0.0625	±5	28181-345-01
R101	1M	Chip	0.0625	±5	28181-345-01
R102	100k	Chip	0.0625	±5	28181-225-01
R103	1M	Metal Oxide	0.25	±5	24141-345-01
R104	10	Chip	0.0625	±5	28181-225-01
R105	270	Metal Oxide	0.25	±2	24141-259-02
R106	100k	Chip	0.0625	±5	28181-321-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors (farads)			V		
C1	1n	Chip, Ceramic	50	±10	28758-253-00
C2	1n	Chip, Ceramic	50	±10	28758-253-00
C3	470n	Electrolytic, Tantalum	35	±20	28575-258-08
C4	10p	Chip, Ceramic	50	±5	28754-025-01
C5	10n	Chip, Ceramic	10	±10	28758-025-00
C6	47n	Chip, Ceramic	50	±10	28758-033-00
C7	10n	Chip, Ceramic	10	±10	28758-025-00
C8	4µ7	Electrolytic, Tantalum	16	±20	28575-134-08
C9	470p	Chip, Ceramic	50	±5	28758-165-01
C10	47n	Chip, Ceramic	50	±10	28758-033-00
C11	22µ	Electrolytic, Tantalum	10	±20	28575-092-08
C12	470p	Chip, Ceramic	50	±5	28758-165-01
C13	1n	Chip, Ceramic	50	±10	28758-253-00
C14	180p	Chip, Ceramic	50	±5	28758-165-01
C15	1n	Chip, Ceramic	50	±10	28758-253-00
C16	220n	Chip, Ceramic	50	±10	28758-041-00
C17	1n	Chip, Ceramic	50	±10	28758-253-00
C18	2µ2	Electrolytic, Tantalum	12	±20	28575-080-08
C19	27p	Chip, Ceramic	50	±5	28758-135-01
C20	4p7	Chip, Ceramic	50	0p5	28754-017-05
C21	1n	Chip, Ceramic	50	±10	28758-253-00
C22	1n	Chip, Ceramic	50	±10	28758-253-00
C23	180p	Chip, Ceramic	50	±5	28758-165-01
C24	180p	Chip, Ceramic	50	±5	28758-165-01
C25	47n	Chip, Ceramic	50	±10	28758-033-00
C26	1n	Chip, Ceramic	50	±10	28758-253-00
C27	1n	Ceramic	100	±5	28718-025-01
C28	47n	Chip, Ceramic	50	±10	28758-033-00
C29	470p	Chip, Ceramic	50	±5	28758-165-01
C30	10p	Chip, Ceramic	50	0p5	28754-025-01
C31	10n	Chip, Ceramic	50	±10	28758-025-00
C32	82p	Chip, Ceramic	50	±5	28758-147-01
C33	47n	Chip, Ceramic	50	±10	28758-033-00
C34	1n	Chip, Ceramic	50	±10	28758-253-00
C35	33p	Chip, Ceramic	50	±5	28758-137-01

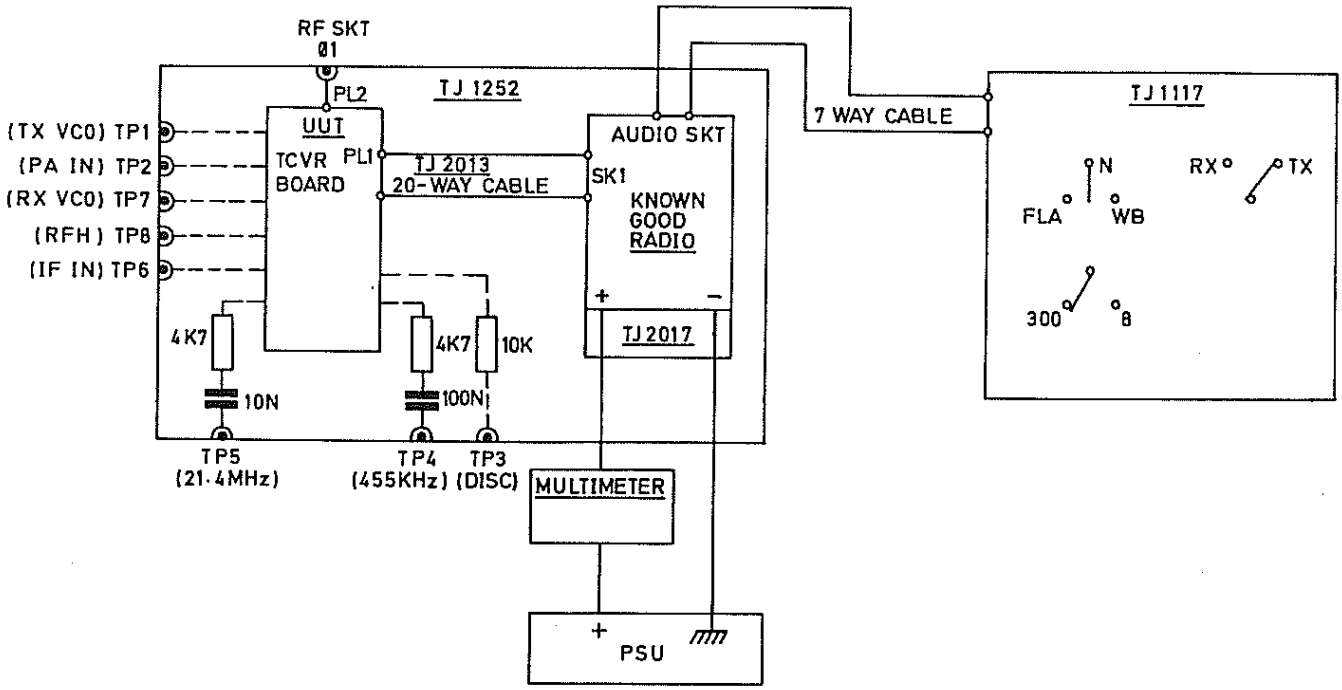
Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C36	47n	Chip, Ceramic	50	±10	28758-033-00
C37	4p7	Chip, Ceramic	50	0p5	28754-017-05
C38	47n	Chip, Ceramic	50	±10	28758-033-00
C39	2p5-10p	Presettable, Ceramic	25		28871-018-00
C40	Not used				
C41	47n	Chip, Ceramic	50	±10	28758-033-00
C42	47n	Chip, Ceramic	50	±10	28758-033-00
C43	2p5-10p	Presettable, Ceramic	25		28871-018-00
C44	22µ	Electrolytic, Tantalum	10	±20	28575-092-08
C45	1n	Chip, Ceramic	50	±10	28758-253-00
C46	15p	Chip, Ceramic	50	±5	28754-029-01
C47	1n	Chip, Ceramic	50	±10	28758-253-00
C48	47n	Chip, Ceramic	50	±10	28758-033-00
C49	8p2	Chip, Ceramic	50	0p5	28754-023-05
C50	10n	Ceramic	100	±10	28751-565-00
C51	10n	Chip, Ceramic	50	±10	28758-025-00
C52	1n	Chip, Ceramic	50	±10	28758-253-00
C53	47n	Chip, Ceramic	50	±10	28758-033-00
C54	10n	Chip, Ceramic	50	±10	28758-025-00
C55	10n	Chip, Ceramic	50	±10	28758-025-00
C56	4n7	Chip, Ceramic	50	±10	28758-021-00
C57	47n	Chip, Ceramic	50	±10	28758-033-00
C58	4n7	Chip, Ceramic	50	±10	28758-021-00
C59	1n	Chip, Ceramic	50	±10	28758-253-00
C60	5p6	Chip, Ceramic	50	0p5	28754-019-05
C61	10n	Chip, Ceramic	50	±10	28758-025-00
C62	3n3	Chip, Ceramic	50	±5	28758-185-01
C63	6n8	Chip, Ceramic	50	±5	28758-263-01
C64	39p	Chip, Ceramic	50	±5	28754-039-01
C65	Part of track				
C66	39p	Chip, Ceramic	50	±5	28754-039-01
C67	10n	Ceramic	50	±5	28751-423-01
C68	10n	Ceramic	100	±10	28751-565-00
C69	10n	Ceramic	50	±5	28751-423-01
C70	39p	Chip, Ceramic	50	±5	28754-039-01
C71	1n	Chip, Ceramic	50	±10	28758-253-00
C72	10n	Chip, Ceramic	50	±5	28758-264-01
C73	10n	Chip, Ceramic	50	±10	28758-025-00
C74	1n	Chip, Ceramic	50	±10	28758-253-00
C75	1n5	Chip, Ceramic	50	±5	28758-177-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C76	15p	Chip, Ceramic	50	±5	28754-029-01
C77	1n	Chip, Ceramic	50	±10	28758-253-00
C78	6p8	Chip, Ceramic	50	0p5	28754-021-05
C79	470p	Chip, Ceramic	50	±5	28758-165-01
C80	22µ	Electrolytic	16	±20	28575-142-08
C81	47n	Chip, Ceramic	50	±10	28758-033-00
C82	1n	Chip, Ceramic	50	±10	28758-253-00
C83	1n	Chip, Ceramic	50	±10	28758-253-00
C84	6p8	Chip, Ceramic	50	0p5	28754-021-05
C85	3n9	Chip, Ceramic	50	±10	28758-020-00
C86	1n	Chip, Ceramic	50	±10	28758-253-00
C87	1n	Chip, Ceramic	50	±10	28758-253-00
C88	33p	Chip, Ceramic	50	±5	28758-137-01
C89	1n	Chip, Ceramic	50	±10	28758-253-00
C90	Part of track				
C91	2p7	Chip, Ceramic	50	0p5	28758-111-05
C92	1n	Chip, Ceramic	50	±10	28758-253-00
C93	6p8	Chip, Ceramic	50	0p5	28754-021-05
C94	1n	Chip, Ceramic	50	±10	28758-253-00
C95	1n	Chip, Ceramic	50	±10	28758-253-00
C96	1n	Chip, Ceramic	50	±10	28758-253-00
C97	10n	Chip, Ceramic	50	±10	28758-025-00
C98	1n	Chip, Ceramic	50	±10	28758-253-00
C99	1n	Chip, Ceramic	50	±10	28758-253-00
C100	39p	Chip, Ceramic	50	±5	28754-039-01
C101	1n5	Chip, Ceramic	50	±10	28758-015-00
C102	270p	Chip, Ceramic	50	±5	28758-159-01
C103	1n	Chip, Ceramic	50	±10	28758-253-00
Inductors and Transformers					
L1		Inductor, Variable, 455kHz		±10	27241-001-00
L2	0.1µH	Inductor		±10	27211-801-00
L3	0.1µH	Inductor		±10	27211-801-00
L4	18µH	Inductor		±10	27211-828-00
L5		Inductor, Variable, 455kHz		±10	27241-001-00
L6	6.8µH	Inductor		±10	27211-823-00
L7	-	Inductor			39280-652-10
L8	0.68µH	Inductor		±10	27211-811-00
L9	5.6µH	Inductor		±10	27211-822-00
L10	0.68µH	Inductor		±10	27211-811-00



TH7158

PRM 4515U : Exploded View Fig.9.1



RACAL
TH 7158

Test Equipment Configuration for
Transceiver Board Alignment

Fig.4.17

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
		VOLUME SWITCH BOARD ASSEMBLY (49280-126-10)			
Resistors (ohms)			**W**		
R1	1M	Chip	0.0625	±5	28181-345-01
R2	1M	Chip	0.0625	±5	28181-345-01
R3	1M	Chip	0.0625	±5	28181-345-01
R4	1M	Chip	0.0625	±5	28181-345-01
R5	1M	Chip	0.0625	±5	28181-345-01
R6	1M	Chip	0.0625	±5	28181-345-01
R7	1M	Chip	0.0625	±5	28181-345-01
R8	1M	Chip	0.0625	±5	28181-345-01
Miscellaneous					
		Sub-Miniature Socket (Special) (6 used)			712419-00000
		6-Way Film Wire			712447-00001
		DECOUPLING (AUDIO) BOARD ASSEMBLY (49280-113-10)			
Capacitors (farads)			**V**		
C1	270p	Chip, Ceramic	50	±5	28758-159-01
C2	270p	Chip, Ceramic	50	±5	28758-159-01
C3	270p	Chip, Ceramic	50	±5	28758-159-01
C4	270p	Chip, Ceramic	50	±5	28758-159-01
C5	270p	Chip, Ceramic	50	±5	28758-159-01
C6	270p	Chip, Ceramic	50	±5	28758-159-01
Inductors					
L1-L13	0.1µH	Inductor, RF		±10	27211-911-00

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
		CHANNEL SWITCH BOARD ASSEMBLY (49280-128-10)			
Resistors (ohms)			W		
R1	1M	Chip	0.0625	±5	28181-345-01
R2	1M	Chip	0.0625	±5	28181-345-01
R3	1M	Chip	0.0625	±5	28181-345-01
R4	1M	Chip	0.0625	±5	28181-345-01
R5	100k	Chip	0.0625	±5	28181-321-01
R6	100k	Chip	0.0625	±5	28181-321-01
R7	100k	Chip	0.0625	±5	28181-321-01
R8	100k	Chip	0.0625	±5	28181-321-01
Miscellaneous					
		Sub-Miniature Socket (Special) (6 Used)			712419-00000
		6-Way Film Wire			712447-00001
		MODE SWITCH BOARD ASSEMBLY (49280-124-10)			
Resistors (ohms)			W		
R1	1M	Chip	0.0625	±5	28181-345-01
R2	1M	Chip	0.0625	±5	28181-345-01
R3	1M	Chip	0.0625	±5	28181-345-01
R4	100k	Chip	0.0625	±5	28181-321-01
R5	100k	Chip	0.0625	±5	28181-321-01
R6	100k	Chip	0.0625	±5	28181-321-01
Miscellaneous					
		Sub-Miniature Socket (Special) (6 Used)			712419-00000
		6-Way Film Wire			712447-00001

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Plugs and Sockets					
PL1		Connector Pin, 20 used			26181-854-01
PL2		50 ohm RF Connector			26272-635-00
Miscellaneous					
FB1		Ferrite Bead			27275-004-03
FB2		Ferrite Bead			27275-004-03
FL1		Ceramic Filter, Four Pole, 455 kHz			27372-011-00
FL2		Crystal Filter, Six Pole, 21.4 MHz			712153-00000
ML1		Double Balanced Mixer			27511-003-00
XL1		Crystal, 6.4 MHz			27371-020-00
XL2		Crystal, 21.855 MHz			27371-021-00
		Screening Can			39280-694-10
		Screening Can			39280-690-10
		Screening Can			39280-692-10

Helical Filters and VCO Modules

NOTE 1:
The following components vary with frequency range covered.

NOTE 2:
Tx Time Out and Frequency Band Selection programmed with links as shown in Tables 2 and 3 (Para 4-32).

		Racal Part Number		
FREQUENCY RANGE (MHz)	REF	FL3 and FL4 HELICAL FILTER	RX VCO (4b) MODULE	TX VCO (4c) MODULE
403-423	A	27241-010-00	49301-174-01	49301-150-01
407-427	B	-010-00	-176-02	-152-02
411-431	C	-011-00	-178-03	-154-03
415-435	D	-011-00	-180-04	-156-04
419-439	E	-011-00	-182-05	-158-05
423-443	F	-012-00	49301-184-06	49301-160-06
427-447	G	-012-00	49280-144-10	49280-146-10
431-451	H	-002-00	49301-186-08	49301-162-08
435-455	J	-002-00	-188-09	-164-09
439-459	K	-002-00	-190-10	-166-10
443-463	L	-008-00	-192-11	-168-11
447-467	M	-008-00	-194-12	-170-12
451-471	N	-008-00	49301-196-13	49301-172-13

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
		CONTROL BOARD ASSEMBLY 2 (49280-118-10)			
		Control Board (PECA)			49280-120-10
SK3		Mode Switch Board Assy (with Flexible Connector)			49280-124-10
SK4		Channel Switch Board Assy (with Flexible Connector)			49280-128-10
SK5		Volume Switch Board Assy (with Flexible Connector)			49280-126-10
SK6		Socket Decoupling Board Assy (with Flexible Connector)			49280-113-10
		CONTROL BOARD A (49280-120-10)			
Resistors (ohms)			W		
R1	1M	Chip	0.0625	±5	28181-345-01
R2	2k2	Chip	0.0625	±5	28181-281-01
R3	100k	Chip	0.0625	±5	28181-321-01
R4	Not used				
R5	100k	Chip	0.0625	±5	28181-321-01
R6	100k	Variable		±10	28361-021-00
R7	100k	Chip	0.0625	±5	28181-321-01
R8	100k	Chip	0.0625	±5	28181-321-01
R9	100k	Chip	0.0625	±5	28181-321-01
R10	1M	Chip	0.0625	±5	28181-345-01
R11	180k	Chip	0.0625	±5	28181-327-01
R12	1k	Chip	0.0625	±5	28181-273-01
R13	50k	Variable		±10	28361-019-00
R14	150k	Chip	0.0625	±5	28181-325-01
R15	1M	Chip	0.0625	±5	28181-345-01
R16	4k7	Chip	0.0625	±5	28181-289-01
R17	22k	Chip	0.0625	±2	28181-305-02
R18	10k	Chip	0.0625	±5	28181-297-01
R19	390k	Chip	0.0625	±5	28181-335-01
R20	120k	Chip	0.0625	±5	28181-323-01
R21	3k3	Chip	0.0625	±5	28181-285-01
R22	470k	Chip	0.0625	±5	28181-337-01
R23	1M	Chip	0.0625	±5	28181-345-01
R24	100k	Chip	0.0625	±5	28181-321-01
R25	1M	Chip	0.0625	±5	28181-345-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R26	5.6	Chip	0.125	±5	28181-019-01
R27	82k	Chip	0.0625	±5	28181-319-01
R28	10k	Chip	0.0625	±5	28181-297-01
R29	10k	Chip	0.0625	±5	28181-297-01
R30	Not Used				
R31	Not Used				
R32	Not Used				
R33	100k	Chip	0.0625	±5	28181-321-01
R34	Not Used				
R35	Not Used				
R36	Not Used				
R37	Not Used				
R38	Not Used				
R39	Not Used				
R40	Not Used				
R41	Not Used				
R42	100k	Chip	0.0625	±5	28181-321-01
R43	1M	Chip	0.0625	±5	28181-345-01
R44	10k	Chip	0.0625	±5	28181-297-01
R45	56k	Chip	0.0625	±2	28181-315-02
R46	4k7	Chip	0.0625	±5	28181-289-01
R47	750k	Chip	0.0625	±5	28181-342-01
R48	100k	Chip	0.0625	±2	28181-321-02
R49	120k	Chip	0.0625	±5	28181-323-01
R50	82k	Chip	0.0625	±5	28181-319-01
R51	1M	Chip	0.0625	±5	28181-345-01
R52	100k	Chip	0.0625	±5	28181-321-01
R53	100k	Chip	0.0625	±5	28181-321-01
R54	220	Chip	0.0625	±5	28181-257-01
R55	1M	Chip	0.0625	±5	28181-345-01
R56	3k3	Chip	0.0625	±5	28181-285-01
R57	100	Chip	0.0625	±5	28181-249-01
R58	4k7	Chip	0.0625	±5	28181-289-01
R59	10k	Chip	0.0625	±5	28181-297-01
R60	100k	Chip	0.0625	±5	28181-321-01
R61	3k3	Chip	0.0625	±5	28181-285-01
R62	470	Chip	0.0625	±5	28181-265-01
R63	120	Chip	0.0625	±5	28181-251-01
R64	390k	Chip	0.0625	±5	28181-335-01
R65	100k	Chip	0.0625	±5	28181-321-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C41	15µ	Electrolytic, Tantalum	20	±20	28585-165-08
C42	1n	Chip, Ceramic	50	±10	28758-013-00
C43	100p	Chip, Ceramic	50	±5	28758-149-01
C44	2µ2	Electrolytic, Tantalum, Bead	10	±20	28574-008-08
Diodes					
D1		1N4099			27711-764-01
D2		1N4617			27711-753-01
D3		1N5817, Schottky			27722-504-00
D4		BAS16			27715-150-00
D5		BZX84C15			27711-872-01
D6		BAS16			27715-150-00
D7		BAS16			27715-150-00
D8		BAS16			27715-150-00
D9		BAS16			27715-150-00
Transistors					
TR1		BSS70, PNP, General Purpose			27761-103-00
TR2		ZVP2106A, FET, P-channel			27771-007-00
TR3		BSS123, FET, N-channel			27771-720-00
TR4		BCX70J, NPN, General Purpose			27763-107-00
TR5		BS250, FET, P-channel			27771-008-00
TR6		BS250, FET, P-channel			27771-008-00
TR7		BCX71J, PNP, General Purpose			27761-102-00
TR8		IFRD9120, FET, P-channel			27771-182-00
TR9		IFRD9120, FET, P-channel			27771-182-00
TR10		BCX71J, PNP, General Purpose			27761-102-00
TR11		BCX71J, PNP, General Purpose			27761-102-00
TR12		BSS123, FET, N-channel			27771-720-00
TR13		BS250, FET, P-channel			27771-008-00
TR14		BCX70J, NPN, General Purpose			27763-107-00
TR15		BCX70J, NPN, General Purpose			27763-107-00
TR16		BCX71J, PNP, General Purpose			27761-102-00
TR17		BCX71J, PNP, General Purpose			27761-102-00
TR18		BCX71J, PNP, General Purpose			27761-102-00
TR19		IFRD9120, FET, P-channel			27771-182-00
TR20		BSS123, FET, N-channel			27771-720-00

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
TR21		BCX38C, Darlington, NPN			27776-001-02
TR22		BSS123, FET			27771-720-00
Integrated Circuits					
ML1		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML2		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML3		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML4		HEF4081BT, Quad 2-Input AND Gates			27821-001-05
ML5		HEF4093BT, Quad 2-Input Schmitt Triggers			27821-709-05
ML6		HEF4001BT, Quad 2-Input NOR Gates			27821-401-05
ML7		Programmed Microprocessor			29839-990-60
ML8		NMC9346, EEPROM			27841-101-00
ML9		HEF4053BT, Triple 2-Channel Multiplexer/ Demultiplexer			27828-604-05
ML10		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML11		PC74HO373, Octal 3-State Latches			27852-373-05
ML12		PC74HO373, Octal 3-State Latches			27852-373-05
ML13		Not Used			
ML14		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML15		LM2903D, Dual Comparators			27816-304-05
ML16		HEF4051BT, 8-Channel Multiplexer/ Demultiplexer			27828-602-05
ML17		HEF4053BT, Triple 2-Channel Multiplexer/ Demultiplexer			27828-604-05
ML18		SL6310C, Mic/Headphone Amp			27813-007-00
Plugs and Sockets					
SK1		20-way Header			26181-909-09
SK2		16-way SIL Socket			26185-017-09
SK7		Jack Connector			26281-523-59
SK40		20-way Socket for ML7			26281-529-59
Miscellaneous					
CR1		Ceramic Resonator, 4MHz			27371-764-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
		CRYPTO BOARD ASSEMBLY A (49280-130-10)			
Resistors (ohms)			W		
R1	10k	Chip	0.0625	±5	28181-297-01
R2	22k	Chip	0.0625	±5	28181-305-01
R3	22k	Chip	0.0625	±5	28181-305-01
R4	10	Chip	0.0625	±5	28181-225-01
R5	10	Chip	0.0625	±5	28181-225-01
R6	270k	Chip	0.0625	±5	28181-331-01
R7	330	Chip	0.0625	±5	28181-261-01
R8	1M	Chip	0.0625	±5	28181-345-01
R9	4k7	Chip	0.0625	±5	28181-289-01
R10	4k7	Chip	0.0625	±5	28181-289-01
R11	270k	Chip	0.0625	±5	28181-331-01
R12	2k7	Chip	0.0625	±5	28181-283-01
R13	4k7	Chip	0.0625	±5	28181-289-01
R14	470	Chip	0.0625	±5	28181-265-01
R15	15k	Chip	0.0625	±5	28181-301-01
R16	47k	Chip	0.0625	±5	28181-313-01
R17	4M7	Chip	0.0625	±10	28181-361-00
R18	47k	Chip	0.0625	±5	28181-313-01
R19	22k	Chip	0.0625	±5	28181-305-01
R20	33k	Chip	0.0625	±5	28181-309-01
R21	330k	Chip	0.0625	±5	28181-333-01
R22	1k	Chip	0.0625	±5	28181-273-01
R23	180k	Chip	0.0625	±5	28181-327-01
R24	22k	Chip	0.0625	±5	28181-305-01
R25	180k	Chip	0.0625	±5	28181-327-01
R26	200k	Thermistor, 7M2003-5, Bead		±5	28251-124-01
R27	150k	Chip	0.0625	±5	28181-325-01
R28	330k	Chip	0.0625	±5	28181-333-01
R29	1M	Variable		±10	28361-026-00
R30	10k	Chip	0.0625	±5	28181-297-01
R31	39k	Chip	0.0625	±5	28181-311-01
R32	39k	Chip	0.0625	±5	28181-311-01
R33	22k	Chip	0.0625	±5	28181-305-01
R34	4k7	Chip	0.0625	±5	28181-289-01
R35	330k	Chip	0.0625	±5	28181-333-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R36	68k	Chip	0.0625	±5	28181-317-01
R37	68k	Chip	0.0625	±5	28181-317-01
R38	390k	Chip	0.0625	±5	28181-335-01
R39	680k	Chip	0.0625	±5	28181-341-01
R40	270k	Chip	0.0625	±5	28181-331-01
R41	1M	Chip	0.0625	±5	28181-345-01
R42	1k	Chip	0.0625	±5	28181-273-01
R43	1k	Chip	0.0625	±5	28181-273-01
R44	100k	Chip	0.0625	±5	28181-321-01
R45	100k	Chip	0.0625	±5	28181-321-01
R46	100k	Chip	0.0625	±5	28181-321-01
R47	1M	Chip	0.0625	±5	28181-345-01
R48	100k	Chip	0.0625	±5	28181-321-01
R49	47k	Chip	0.0625	±5	28181-313-01
R50	470k	Chip	0.0625	±5	28181-337-01
R51	10k	Chip	0.0625	±5	28181-297-01
R52	10k	Chip	0.0625	±5	28181-297-01
R53	47k	Chip	0.0625	±5	28181-313-01
R54	47k	Chip	0.0625	±5	28181-313-01
R55	3M3	Chip	0.0625	±5	28181-357-01
R56	10k	Chip	0.0625	±5	28181-297-01
R57	100k	Chip	0.0625	±5	28181-321-01
R58	10k	Chip	0.0625	±5	28181-297-01
R59	1M	Chip	0.0625	±5	28181-345-01
R60	330k	Chip	0.0625	±5	28181-333-01
R61	180k	Chip	0.0625	±5	28181-327-01
R62	150k	Chip	0.0625	±5	28181-325-01
R63	120k	Chip	0.0625	±5	28181-323-01
R64	120k	Chip	0.0625	±5	28181-323-01
R65	100k	Chip	0.0625	±5	28181-321-01
R66	120k	Chip	0.0625	±5	28181-323-01
R67	120k	Chip	0.0625	±5	28181-323-01
R68	150k	Chip	0.0625	±5	28181-325-01
R69	180k	Chip	0.0625	±5	28181-327-01
R70	330k	Chip	0.0625	±5	28181-333-01
R71	1M	Chip	0.0625	±5	28181-345-01
R72	15k	Chip	0.0625	±5	28181-301-01
R73	15k	Chip	0.0625	±5	28181-301-01
R74	4k7	Chip	0.0625	±5	28181-289-01
R75	4k7	Chip	0.0625	±5	28181-289-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R76	470k	Chip	0.0625	±5	28181-337-01
R77	22k	Chip	0.0625	±5	28181-305-01
R78	27k	Chip	0.0625	±5	28181-307-01
R79	10k	Chip	0.0625	±5	28181-297-01
R80	1M	Chip	0.0625	±5	28181-345-01
R81	12k	Chip	0.0625	±5	28181-299-01
R82	12k	Chip	0.0625	±5	28181-299-01
R83	Not Used				
R84	27k	Chip	0.0625	±5	28181-307-01
R85	100k	Chip	0.0625	±5	28181-321-01
R86	100k	Chip	0.0625	±5	28181-321-01
R87	100k	Chip	0.0625	±5	28181-321-01
R88	100k	Chip	0.0625	±5	28181-321-01
R89	1M	Chip	0.0625	±5	28181-345-01
R90	1M	Chip	0.0625	±5	28181-345-01
R91	1M	Chip	0.0625	±5	28181-345-01
R92	150k	Chip	0.0625	±5	28181-325-01
R93	Not Fitted				
R94	100	Chip	0.0625	±5	28181-249-01
R95	100	Chip	0.0625	±5	28181-249-01
R96	100	Chip	0.0625	±5	28181-249-01
R97	100k	Chip	0.0625	±5	28181-321-01
R98	150k	Chip	0.0625	±5	28181-325-01
R99	10k	Chip	0.0625	±5	28181-297-01
R100	10k	Chip	0.0625	±5	28181-297-01
R101	10k	Chip	0.0625	±5	28181-297-01
R102	10k	Chip	0.0625	±5	28181-297-01
R103	10k	Chip	0.0625	±5	28181-297-01
R104	1M	Chip	0.0625	±5	28181-345-01
R105	1M	Chip	0.0625	±5	28181-345-01
R106	1M	Chip	0.0625	±5	28181-345-01
R107	1M	Chip	0.0625	±5	28181-345-01
R108	470k	Chip	0.0625	±5	28181-337-01
R109	1M	Chip	0.0625	±5	28181-345-01
R110	12k	Chip	0.0625	±5	28181-297-01
R111	1M	Chip	0.0625	±5	28181-345-01
R112	1k	Chip	0.0625	±5	28181-273-01
R113	10k	Chip	0.0625	±5	28181-297-01
R114	1M	Chip	0.0625	±5	28181-345-01
R115	10k	Chip	0.0625	±5	28181-297-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R116	10k	Chip	0.0625	±5	28181-297-01
R117	100k	Chip	0.0625	±5	28181-321-01
R118	47k	Chip	0.0625	±5	28181-313-01
R119	1k5	Chip	0.0625	±5	28181-277-01
Capacitors (farads)			V		
C1	2µ2	Electrolytic, Chip, Tantalum	10	±20	28573-118-08
C2	2µ2	Electrolytic, Chip, Tantalum	10	±20	28573-118-08
C3	15µ	Electrolytic, Chip, Tantalum	10	±20	28573-213-08
C4	15µ	Electrolytic, Chip, Tantalum	10	±20	28573-213-08
C5	15µ	Electrolytic, Chip, Tantalum	10	±20	28573-213-08
C6	33p	Chip, Ceramic	50	±5	28758-137-01
C7	10µ	Electrolytic, Chip, Tantalum	16	±20	28573-217-08
C8	2µ2	Electrolytic, Chip, Tantalum	10	±20	28573-118-08
C9	0µ47	Electrolytic, Chip, Tantalum	20	±20	28573-133-08
C10	2µ2	Electrolytic, Chip, Tantalum	10	±20	28573-118-08
C11	100n	Chip, Ceramic	50	±10	28758-037-00
C12	2µ2	Electrolytic, Chip, Tantalum	10	±20	28573-118-08
C13	0µ47	Electrolytic, Chip, Tantalum	20	±20	28573-133-08
C14	10n	Chip, Ceramic	50	±10	28758-025-00
C15	560p	Chip, Ceramic	50	±10	28758-250-00
C16	1n2	Chip, Ceramic	50	±10	28758-175-00
C17	3n3	Chip, Ceramic	50	±10	28758-185-00
C18	1n2	Chip, Ceramic	50	±10	28758-175-00
C19	390p	Chip, Ceramic	50	±10	28758-163-00
C20	22n	Chip, Ceramic	50	±10	28758-029-00
C21	4n7	Chip, Ceramic	50	±10	28758-189-00
C22	10n	Chip, Ceramic	50	±10	28758-257-00
C23	10n	Chip, Ceramic	50	±10	28758-257-00
C24	10n	Chip, Ceramic	50	±10	28758-257-00
C25	5-35p	Variable, Ceramic, Disc	25		28871-017-00
C26	10p	Chip, Ceramic	50	±5	28758-125-01
C27	10n	Chip, Ceramic	50	±10	28758-025-00
C28	220n	Chip, Ceramic	50	±10	28758-041-00
C29	10n	Chip, Ceramic	50	±10	28758-025-00
C30	0.047	Double Layer	5.5	+80-20	28541-001-09
C31	10n	Chip, Ceramic	50	±10	28758-025-00
C32	1n5	Chip, Ceramic	50	±10	28758-175-00
C33	2n2	Chip, Ceramic	50	±5	28758-181-01
C34	390p	Chip, Ceramic	50	±10	28758-163-00
C35	220n	Chip, Ceramic	50	±10	28758-041-00

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
C36	220n	Chip, Ceramic	50	±10	28758-041-00
C37	220n	Chip, Ceramic	50	±10	28758-041-00
C38	220n	Chip, Ceramic	50	±10	28758-041-00
C39	Not Fitted				
C40	100p	Chip, Ceramic	50	±5	28758-149-01
C41	10n	Chip, Ceramic	50	±10	28758-025-00
C42	10n	Chip, Ceramic	50	±10	28758-025-00
C43	10n	Chip, Ceramic	50	±10	28758-025-00
C44	10n	Chip, Ceramic	50	±10	28758-025-00
C45	1n	Chip, Ceramic	50	±10	28758-013-01
C46	100p	Chip, Ceramic	50	±5	28758-149-01
C47	100p	Chip, Ceramic	50	±5	28758-149-01
C48	10n	Chip, Ceramic	50	±10	28758-025-00
C49	180p	Chip, Ceramic	50	±5	28758-155-01
C50	10n	Chip, Ceramic	50	±10	28758-025-00
C51	1µ	Electrolytic, Chip, Tantalum	10	±20	28573-117-08
C52	3n9	Chip, Ceramic	50	±10	28758-020-00
C53	680p	Chip, Ceramic	50	±10	28758-251-00
C54	18p	Chip, Ceramic	50	±5	28758-131-01
C55	2µ2	Electrolytic, Chip, Tantalum	10	±20	28573-118-08
C56	10n	Chip, Ceramic	50	±10	28758-025-00

Diodes

D1	BAS16, Switching	27715-150-00
D2	BAV99, Switching	27715-129-00
D3	BAV99, Switching	27715-129-00
D4	BAS16, Switching	27715-150-00
D5	BAS16, Switching	27715-150-00
D6	BAS16, Switching	27715-150-00
D7	BAS16, Switching	27715-150-00
D8	BAV99, Switching	27715-129-00
D9	BAS16, Switching	27715-150-00
D10	1N4626	27711-762-01
D11	BAS16, Switching	27715-150-00
D12	BAS16, Switching	27715-150-00
D13	BAS16, Switching	27715-150-00
D14	BAS16, Switching	27715-150-00
D15	BAS16, Switching	27715-150-00

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Transistors					
TR1		BCX70J, NPN, General Purpose			27763-107-00
TR2		BCX71J, PNP, General Purpose			27761-102-00
TR3		BS250, FET, P-channel			27771-008-00
TR4		BS250, FET, P-channel			27771-008-00
TR5		BSS123, FET, N-channel			27771-720-00
TR6		BF511, FET, N-channel			27771-392-00
TR7		BCX71J, PNP, General Purpose			27761-102-00
TR8		BCX70J, NPN, General Purpose			27761-107-00
TR9		BS250, FET, P-channel			27771-008-00
TR10		BCX70J, NPN, General Purpose			27761-107-00
Integrated Circuits					
ML1		NE5534D, Low Noise Op Amp			27811-004-05
ML2		HCT4053T, Triple 2-Channel Multiplexer/ Demultiplexers			27853-053-05
ML3		LM358D, Dual Op Amps			27811-806-05
ML4		LM358D, Dual Op Amps			27811-806-05
ML5		HEF4053BT, Triple 2-Channel Multiplexer/ Demultiplexers			27828-604-05
ML6		HEF4069UBT, Hex Inverters			27828-001-05
ML7		HEF4040BT, 12-Stage Counter/Divider			27824-011-05
ML8		HEF4053BT, Triple 2-Channel Multiplexer/ Demultiplexer			27828-604-05
ML9		Encryption Module			
ML10		HEF4001BT, Quad 2-Input NOR Gates			27821-401-05
ML11		HC1-55564-9 Codec			27818-005-00
ML12		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML13		LM2903D, Dual Comparators			27816-304-05
ML14		RMSL-032, Clock Recovery LSI			27827-041-63
ML15		HEF4015BT, Dual 4-Stage Shift Registers			27825-104-05
ML16		HEF4015BT, Dual 4-Stage Shift Registers			27825-104-05
ML17		MC1776D, Programmable Low-Power Op Amp			27811-013-05
ML18		HEF4040BT, 12-Stage Counter/Divider			27824-011-05
Plugs, Sockets and Miscellaneous					
PL1		Pin Contacts (32 used for PL1)			26181-853-01
		Socket Terminals (30 used for ML9)			26281-090-54
XTL1		Crystal, 4.096 MHz			27371-015-50

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Capacitors (farads)			V		
C1	100n	Chip, Ceramic	50	±10	28758-037-00
C2	47n	Chip, Ceramic	50	±10	28758-061-00
C3	2µ2	Electrolytic, Tantalum, Bead	10	±20	28574-008-08
C4	47µ	Electrolytic, Tantalum	20	±20	28575-171-08
C5	2µ2	Electrolytic, Tantalum, Bead	10	±20	28574-008-08
C6	2µ2	Electrolytic, Tantalum, Bead	10	±20	28574-008-08
C7	100n	Chip, Ceramic	50	±10	28758-037-00
C8	10n	Chip, Ceramic	50	±10	28758-025-00
C9	10n	Chip, Ceramic	50	±10	28758-025-00
C10	10n	Chip, Ceramic	50	±10	28758-025-00
C11	10n	Chip, Ceramic	50	±10	28758-025-00
C12	33p	Chip, Ceramic	50	±5	28758-137-01
C13	33p	Chip, Ceramic	50	±5	28758-137-01
C14	10n	Chip, Ceramic	50	±10	28758-025-00
C15	10n	Chip, Ceramic	50	±10	28758-025-00
C16	10n	Chip, Ceramic	50	±10	28758-025-00
C17	10n	Chip, Ceramic	50	±10	28758-025-00
C18	10n	Chip, Ceramic	50	±10	28758-025-00
C19	10n	Chip, Ceramic	50	±10	28758-025-00
C20	10n	Chip, Ceramic	50	±10	28758-025-00
C21	1n	Chip, Ceramic	50	±10	28758-013-00
C22	Not Used				
C23	22n	Chip, Ceramic	50	±10	28758-029-00
C24	22n	Chip, Ceramic	50	±10	28758-029-00
C25	150n	Chip, Ceramic	50	±10	28758-039-00
C26	680p	Chip, Ceramic	50	±5	28758-251-01
C27	10n	Chip, Ceramic	50	±10	28758-025-00
C28	220n	Chip, Ceramic	50	±10	28758-041-00
C29	10n	Chip, Ceramic	50	±10	28758-025-00
C30	2n2	Chip, Ceramic	50	±10	28758-017-00
C31	100n	Chip, Ceramic	50	±10	28758-037-00
C32	10n	Chip, Ceramic	50	±10	28758-025-00
C33	2µ2	Electrolytic, Tantalum, Bead	10	±20	28574-008-08
C34	10n	Chip, Ceramic	50	±10	28758-025-00
C35	100n	Chip, Ceramic	50	±10	28758-037-00
C36	27p	Chip, Ceramic	50	±5	28758-135-01
C37	22n	Chip, Ceramic	50	±10	28758-029-00
C38	33µ	Electrolytic, Alum.	16	±20	28512-053-08
C39	1µ5	Electrolytic, Tantalum, Bead	16	±20	28574-010-08
C40	100µ	Electrolytic, Tantalum	10	±20	28575-100-08

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
R66	4M7	Chip	0.0625	±10	28181-361-00
R67	4M7	Chip	0.0625	±10	28181-361-00
R68	1M	Chip	0.0625	±5	28181-345-01
R69	1M	Chip	0.0625	±5	28181-345-01
R70	10k	Chip	0.0625	±5	28181-297-01
R71	100k	Chip	0.0625	±5	28181-321-01
R72	39k	Chip	0.0625	±5	28181-311-01
R73	100k	Chip	0.0625	±5	28181-321-01
R74	100k	Chip	0.0625	±5	28181-321-01
R75	100k	Chip	0.0625	±5	28181-321-01
R76	1M	Chip	0.0625	±5	28181-345-01
R77	10k	Chip	0.0625	±5	28181-297-01
R78	47k	Chip	0.0625	±5	28181-313-01
R79	1M	Chip	0.0625	±5	28181-345-01
R80	180k	Chip	0.0625	±5	28181-327-01
R81	220k	Chip	0.0625	±5	28181-329-01
R82	10k	Chip	0.0625	±5	28181-297-01
R83	0	Chip			28181-200-00
R84	220k	Chip	0.0625	±5	28181-329-01
R85	0	Chip			28181-200-00
R86	27k	Chip	0.0625	±2	28181-307-02
R87	100k	Chip	0.0625	±5	28181-321-01
R88	220k	Chip	0.0625	±5	28181-329-01
R89	470k	Chip	0.0625	±5	28181-337-01
R90	1M	Chip	0.0625	±5	28181-345-01
R91	62k	Chip	0.0625	±2	28181-316-02
R92	1M	Chip	0.0625	±5	28181-345-01
R93	120k	Chip	0.0625	±5	28181-323-01
R94	470k	Chip	0.0625	±5	28181-337-01
R95	18k	Chip	0.0625	±5	28181-303-01
R96	270k	Chip	0.0625	±2	28181-331-02
R97	Not Fitted				
R98	6k8	Chip	0.0625	±5	28181-293-01
R99	1M	Chip	0.0625	±5	28181-345-01
R100	1M	Chip	0.0625	±5	28181-345-01
R101	22k	Chip	0.0625	±2	28181-305-02
R102	270k	Chip	0.0625	±2	28181-331-02
R103	150k	Chip	0.0625	±5	28181-325-01

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
L11	10µH	Inductor		±10	27211-825-00
L12	0.047µH	Inductor		±10	27211-906-00
L13	-	Inductor			39280-652-10
L14	10µH	Inductor		±10	27211-825-00
L15	0.68µH	Inductor		±10	27211-811-00
L16	10µH	Inductor		±10	27211-825-00
L17	-	Inductor			39280-652-10
L18	0.68µH	Inductor		±10	27211-811-00
L19	-	Inductor			39280-653-10
L20	-	Inductor			39280-656-10
L21	0.033µH	Inductor		±10	27211-910-00
L22	0.047µH	Inductor		±10	27211-906-00
L23	0.18µH	Inductor		±10	27211-804-00
L24	0.027µH	Inductor		±10	27211-912-00
L25	0.68µH	Inductor		±10	27211-811-00
L26	0.033µH	Inductor		±10	27211-910-00
L27	0.68µH	Inductor		±10	27211-811-00
L28	0.1µH	Inductor		±10	27211-911-00
L29	0.68µH	Inductor		±10	27211-811-00
L30	0.68µH	Inductor		±10	27211-811-00
L31	0.1µH	Inductor		±10	27211-911-00
T1		Transformer			49280-280-10
Diodes					
D1		BBY40, Tuning, 28V			27721-246-00
D2		BAS16, Switching, 85V			27715-150-00
D3		BAS16, Switching, 85V			27715-150-00
D4		BAS16, Switching, 85V			27715-150-00
D5		BAS16, Switching, 85V			27715-150-00
D6		BAS16, Switching, 85V			27715-150-00
D7		BAV99, Switching, 70V			27715-129-00
D8		MA4P274, Pin			27722-020-00
D9		BAT18, Pin, 35V			27722-019-00
D10		BAT17, Schottky, 4V			27722-508-00
D11		BAT18, Pin, 35V			27722-019-00
D12		MA4P274, Pin			27722-020-00

Cct. Ref.	Value	Description	Rat.	Tol. %	Racal Part Number
Transistors					
TR1		BCX70J, NPN, General Purpose			27763-107-00
TR2		BFS17, NPN, VHF			27763-101-01
TR3		BCX70J, NPN, General Purpose			27763-107-00
TR4		BCX70J, NPN, General Purpose			27763-107-00
TR5		BCX70J, NPN, General Purpose			27763-107-00
TR6		BFR92, NPN, UHF			27763-007-00
TR7		BCX71J, PNP, General Purpose			27761-102-00
TR8		BFR93, NPN, UHF			27763-009-00
TR9		BFT92, PNP, UHF			27761-104-00
TR10		BF689K, NPN, General Purpose			27763-106-00
TR11		ZTX752, PNP, General Purpose			27765-052-00
TR12		BFR92A, NPN, UHF			27763-007-01
TR13		BCX70J, NPN, General Purpose			27763-107-00
TR14		BFT92, PNP, UHF			27761-104-00
TR15		BF689K, NPN, General Purpose			27763-106-00
TR16		MRF750, NPN, Power, RF			27767-110-00
TR17		N-channel FET			711676-00000
TR18		MRF752, NPN, Power, RF			27767-111-00
TR19		BFR93A, NPN, UHF			27763-009-01
TR20		ZTX109, NPN, General Purpose			27763-312-00
TR21		BCX70J, NPN, General Purpose			27763-107-00
TR22		BSS250, P-channel FET			27771-008-00
TR23		BSS123, N-channel FET			27771-720-00
TR24		BSS250, P-channel FET			27771-008-00
TR25		IRFD9120, P-channel FET			27771-182-00
TR26		BSS123, N-channel FET			27771-720-00
Integrated Circuits					
IC1		MC3357P, FM IF System			27814-703-00
IC2		SP8719, Divider 80/ 81			27824-021-03
IC3		BCC024, Synthesiser			27827-024-53
IC4		LM2904D, Dual Op Amps			27811-806-05
IC5		HEF4021BT, Eight-bit Shift Register			27825-151-05

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