

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series 512 and 1024 bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

FEATURES

- HIGH FREQUENCY OPERATION – 5MHz TYPICAL
- SINGLE 512, SINGLE 1024
- TTL, DTL COMPATIBLE
- WRITE AND READ CONTROLS INCLUDED
- LOW POWER DISSIPATION – 200 μ W/BIT AT 1 MHz
- +5, -5 POWER SUPPLIES
- STANDARD PACKAGE 8-LEAD DIP
- P-MOS SILICON GATE TECHNOLOGY

APPLICATIONS

- FAST ACCESS SWAPPING MEMORY SYSTEMS
- LOW COST SEQUENTIAL ACCESS MEMORIES
- LOW COST BUFFER MEMORIES
- CRT REFRESH MEMORIES
- RELAY LINE MEMORY REPLACEMENT
- DRUM MEMORY REPLACEMENT

PROCESS TECHNOLOGY

Use of low threshold silicon gate technology allows high speed (5MHz typical) while reducing power dissipation and clock input capacitance dramatically as compared to other technologies. The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

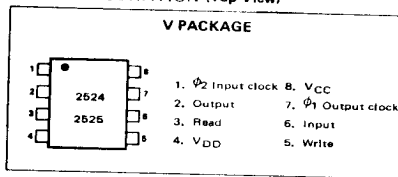
POLAR COMPATIBILITY

The signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The bare drain output stage provides driving capability for both MOS and bipolar integrated circuits (standard TTL load).

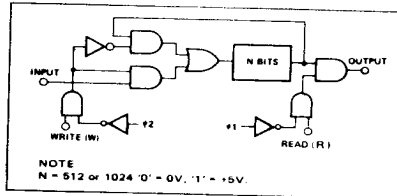
SILICONE PACKAGING

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read Mode, Output is Data

PART IDENTIFICATION TABLE

PART NO.	BIT LENGTH	PACKAGE
2524V	512	8 pin DIP
2525V	1024	8 pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2) 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Power Dissipation (2) 535mW@T_A>70°C
 Data and Clock Input Voltages and Supply Voltages with respect to V_{CC} +0.3V to -20V

2. For operating at elevated temperature the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. See "Minimum Operating Frequency" graph for low limits on data rate.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Parameters are valid over operating temperature range unless otherwise specified.
9. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.
10. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OL} and V_{CLAMP} and the value of the pull-down resistor (R_L).

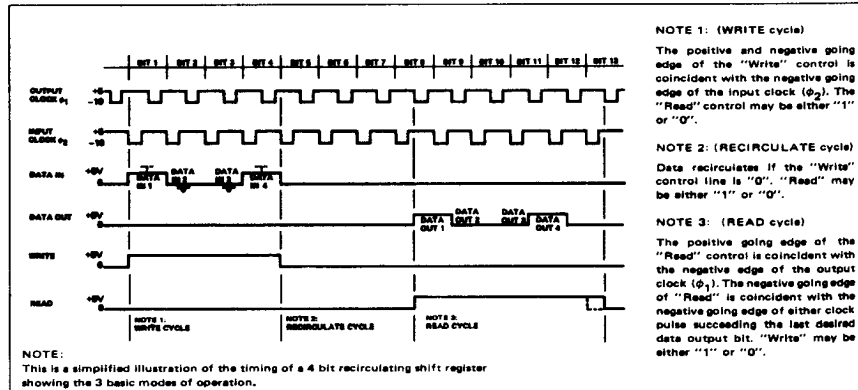
NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = -5V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYPICAL	MAX	UNIT	CONDITION
I _{LI}	Input Load Current		10	500	nA	V _{IN} = -5.5V; T _A = 25°C
I _{LO}	Output Leakage Current		10	1000	nA	V _{φ1} = V _{φ2} = -12V; V _{DD} = -5V V _{OUT} = -5.5V; T _A = 25°C
I _{LC}	Clock Leakage Current		10	1000	nA	V _{ILC} = -12V ; T _A = 25°C
I _{DD}	Power Supply Current: 2524		15	35	mA	Continuous Operation; φpW = 150ns; f = 1 MHz V _{ILC} = -12V; T _A = 25°C V _{DD} = -5.5V
		2525	25	35	mA	
V _{IL}	Input "Low" Voltage	-5.0		+0.6	V	Note 9
V _{IH}	Input "High" Voltage	+3.4		5.3	V	Note 9
V _{ILC}	Clock Input "Low" Voltage	-12.0		-10.0	V	
V _{IHC}	Clock Input "High" Voltage	4.0		5.3	V	

EXAMPLE TIMING DIAGRAM

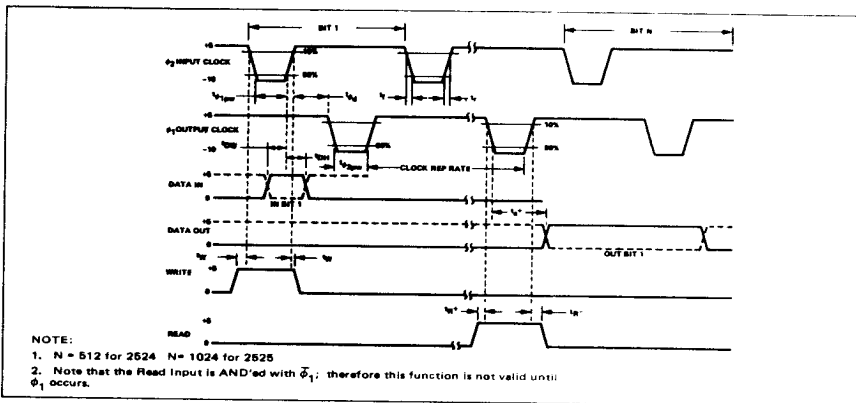


SIGNETICS 512 AND 1024 BIT RECIRCULATING DYNAMIC SHIFT REGISTERS ■ 2524, 2525

CONDITIONS OF TEST

Input rise and fall times: 10 sec Output load is 1 TTL gate

TIMING DIAGRAM

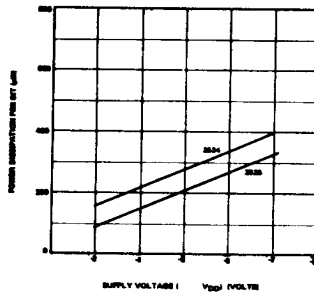


AC CHARACTERISTICS $T_A = +25^\circ\text{C}$ $V_{CC} = +5\text{V} \pm 5\%$; $V_{DD} = -5\text{V} \pm 5\%$; $V_{ILC} = -11\text{V}$

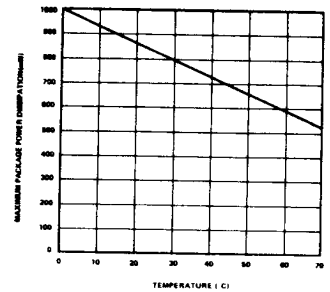
SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Data Rep Rate	.0005 (Note 4)	5	3	MHz	$W = R = V_{CC}$
t_{pw}	Clock Pulse Width	135	85		ns	
t_{pd}	Clock Pulse Delay	10			ns	
t_r, t_f	Clock Pulse Transition	10		1000	ns	
t_{pw}	Data Write (Setup) Time	70			ns	
t_{DH}	Data to Clock Hold Time	20			ns	
t_{g+}	Clock to Data Out Delay			100	ns	
t_{R-} ; t_{W-}	Clock to "Read" or "Write" Timing	0			ns	
t_{R+} ; t_{W+}	Clock to "Read" or "Write" Timing	0			ns	
C_{in}	Input Capacitance			5	pF	1MHz; $V_I = V_{CC}$; $V_{AC} = 25\text{m V}_{p,p}$
C_{out}	Output Capacitance			5	pF	1MHz; $V_O = V_{CC}$; $V_{AC} = 25\text{m V}_{p,p}$
C_ϕ	Clock Capacitance			80 160	pF pF	1MHz; $V = V_{CC}$; $V_{AC} = 25\text{m V}_{p,p}$
V_{OL}	Output "Low" Voltage		-1.0		v	$R_L = 3.0\text{K}$; 1 TTL Load ($I_L = 1.6\text{mA}$) Note 10
V_{OHI}	Output "High" Voltage Driving 1 TTL Load	2.4	3.5		V	$R_L = 3.0\text{K}$; 1 TTL Load ($I_L = 100\mu\text{A}$)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4.0		V	$R_L = 5.6\text{K}$; $C_L = 10\text{pF}$

CHARACTERISTIC CURVES

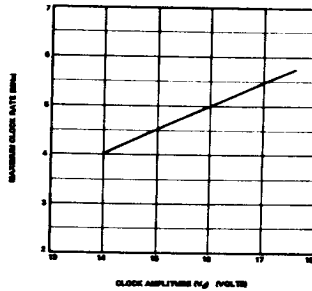
POWER DISSIPATION/BIT
VERSUS SUPPLY VOLTAGE



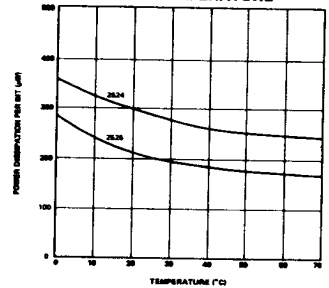
MAXIMUM PACKAGE POWER
DISSIPATION VERSUS TEMPERATURE



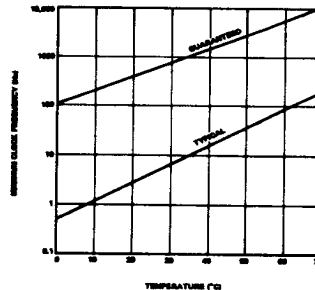
MAXIMUM CLOCK RATE
VERSUS CLOCK AMPLITUDE



POWER DISSIPATION/BIT
VERSUS TEMPERATURE



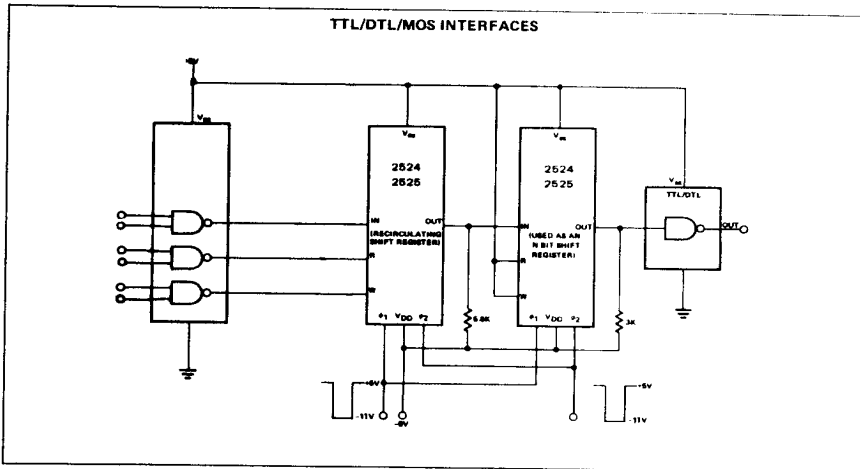
MINIMUM OPERATING CLOCK
FREQUENCY VERSUS TEMPERATURE



NOTE:

Conditions for typical curves: V_{CC} = +5V, V_{DD} = -5V, clock duty cycle = 35%, t_{CLK} = 3MHz, V_{DD-P} = 16V, φ_{FW1} = φ_{FW2} = 80ns, T_A = +25°C unless otherwise noted.

APPLICATIONS DATA



CIRCUIT SCHEMATIC

