FAULTFINDING INSTRUCTIONS for CRYPTOMODULE OF AROFLEX TRAINING MANUAL

APPENDICES

PHILIPS

Philips Usfa B.V.

Faultfinding Instructions

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1. SAFETY

Read this page carefully before installation and use of the instrument.

1.1 INTRODUCTION

The instrument described in this manual is designed to be used by properly-trained personnel only.
Adjustment, maintenance and repair of the exposed equipment shall be carried out only by qualified personnel who are aware of the hazards involved.

1.2 SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and servicing personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual. Specific warning and caution statements, where they apply, will be found throughout the manual.
Where necessary, warning and caution statements and/or symbols are marked on the apparatus.

1.3 CAUTION AND WARNING STATEMENTS

CAUTION is used to indicate correct operating or maintenance procedures in order to prevent damage to or destruction of equipment or other property.
WARNING calls attention to a potential danger that requires correct procedures or practices in order to prevent personal injury.

1.4 SYMBOLS

Read the operating instructions

1.5 IMPAIRED SAFETY-PROTECTION

Whenever it is likely that safety-protection has been impaired, the instrument **must** be made inoperative and be secured against any unintended operation. The matter should then be referred to the appropriate servicing authority.
Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

2. GENERAL INFORMATION

The Logic Multimeter PM 2544 combines the traditional multimeter measurements of all standard electrical parameters including frequency, time and peak, with a 'signature analysis' facility for data-flow comparison, making it the ideal tool for measurements in digital cicuits.

Other facilities include autoranging, a relative reference mode for comparison checks, and overload protection with visual and audible indication.

The instrument is intended for mains operation from a nominal 220 V, 50 Hz supply, but can be adapted to other mains input voltages.
In the signature analysis function, signatures are checked against normal listing in documentation or against a preloaded plug-in memory.

As an aid to understanding the various functions and facilities provided by the logic multimeter, these are briefly outlined in the following subsections.

2.1 SIGNATURE ANALYSIS

Briefly, signature analysis can be described as a data-flow comparison technique that enables the testing of microprocessor-controlled and other digital equipment down to component level.
The signature is a serial data flow of any length compressed to a single 4-bit character code, which enables the presence of the correct signal to be checked at any point in the circuit under test. Due to the method of compressing, and the fact that a 4-bit character code in hexadecimal can contain up to 65,536 different values, the signatures obtained can each be considered as unique.

To assure reproduceable conditions, 'start' and 'stop' pulses (for defining the time period) and the clock pulse are taken from the circuit under test, which is running in a defined routine.

To enable different types of logic circuits to be tested the high and low levels are settable for data input as well as for start, stop and clock signal. Also the edge of last signals can be selected for maximum freedom and performance.

A 'qualifier' function is available to eliminate certain parts in the signal flow that cannot be reproduced and should therefore be neglected in composing the signature.

The standard method of working with signature analysis is to compare the signatures found in circuit with the ones listed for the different modes in the documentation.

However, the Philips PM 2544 offers the additional feature of storing the signatures in plug-in memory modules to facilitate testing. Each memory module is loaded by making measurements on a correctly-functioning instrument and can then be subsequently used for testing identical instruments.
The memory modules are compact and easy to exchange.

2.1.1 Taking a Signature

Signatures are captured in the free-running or hold mode from the signal sampled by the data probe under the control of the start, stop and clock and, if necessary, the qualifier signals sampled by the pod (see Section 6.3).
The signatures are displayed if four hexadecimal characters (0 to 9 and ACFHPU).
Unstable signatures are marked by '~'. In the 'latch unstable signature' mode, unstable signatures can be captured out of a continuous stream of data and displayed.

2.1.2 Signal Levels

The trigger levels of the data probe and pod can be independently set to either TTL or VAR(iable). In the variable position the data probe high and low levels and the pod level can be independently set between + 12.7 V and – 12.7 V. The default levels for VAR (at switching on) are for CMOS 5 V logic. All trigger levels can be displayed. The trigger edges of start, stop and clock and the qualifier high or low level can be selected.

2.1.3 Data Probe with Logic-State Indicator

The data probe carries a pushbutton switch and a LED indicator for the 'hold' mode and a second LED to indicate low, high or undefined for the logic state. Small pulse are shown via a pulse stretcher.

2.2 MEMORY MODULE OPTION

An optional feature consists of a module holder that can be attached to an instrument to accommodate plug-in memory modules for long-term storage of 125 signatures per module. Such a module may be loaded with signatures and preset values for trigger level and trigger edges by making measurement on the first memory location in the 'store' mode. Later, measured signatures may be compared with the stored in a memory. An incorrect signature is indicated by an error (E) in the display accompanied by two audible alarm signals. A correct signature is indicated with one audible signal.

2.3 OTHER LOGIC FUNCTIONS

Several other measuring functions can be made via the data probe including peak voltages and frequency measurements. In conjunction with the start and stop inputs, time measurements and event counting are also possible.
Briefly these facilities comprise:

Peak Voltage
Positive or negative peaks with a minimum pulse-width of 20 ns (at repetition rates of 20 Hz minimum) can be measured with 0,1 V resolution in the range between + 12.6 V and – 12.6 V.

Frequency

Frequency is measured in four ranges up to 20 MHz maximum on a 5-digit display, with auto-ranging. The trigger level is settable as for signatures.

Time Measurement

The time interval between the start and stop signals can be measured in eight ranges (with auto-ranging) between 100 ns resolution and 10^5s. The minimum pulse width of start and stop pulses is 100 ns. Trigger levels are settable as for signatures.

Event Counting

The number of low to high transitions during a gate time defined by the start and stop pulses are counted up to a maximum of 10^{11} counts with a resolution of 5 digits. The minimum time spacing between two counts is 50 ns. Event counting is an automatic function using auto-ranging.

Overload Protection

The data probe and pod inputs are protected against voltage overloads of 150 V a.c. or d.c. continuously, and 250 V a.c. or d.c. for maximum of 10 seconds, with a maximum of 350 V peak.
The ground is floating with respect to earth. Maximum common mode voltage 30 Vrms, 42.4 V peak.

2.4 STANDARD MULTIMETER FUNCTIONS

The standard functions for voltage, current and resistance measurements are available with overload protection and relative reference facilities.

Voltages

Voltage measurements with manual or auto-ranging can be made to a maximum of 450 V with a resolution of 100 μV max. on a 5-digit display (with 10% overrange). The a.c. measurements are a.c. coupled r.m.s. with a bandwidth of 20 kHz.

DC currents

Two ranges (100 mA and 10 A) are used for d.c. current measurements on a 5-digit display (with 10% overranges). The 100 mA range is fuse-protected.

Resistance Measurements

Resistance values between 0,1Ω resolution and 10 MΩ full-scale are measured in five manual or automatic ranges. Continuity tests can be performed in all resistance ranges in the manual-ranging mode, a sound singnal being produced at display values less than 100.

Relative Reference Mode (zero set)

If necessary, voltage, current and resistance can be measured in the relative reference mode, where each measured value may be stored as a reference value. In this mode, successive measurements are indicated as positive or negative deviations from the stored value. A required reference value can also be set manual on the instrument.

Overload Protection

An overload occurring on voltage or current ranges is indicated visually by 'OL' on the display. The voltage ranges are protected against overloads up to 450 Vrms: the resistance ranges are protected up to 250 Vrms input. An audible warning is given in case of $>$ 450 V in the highest range of the voltage functions and $>$ 110 mA and 11 A in the current functions.

3. CHARACTERISTICS

3.1 PERFORMANCE CHARACTERISTICS

Properties expressed in numerical values with stated tolerances are guaranteed by **N.V. Philips' Gloeilampenfabrieken.** Specified non-tolerance numerical values indicate those that could be **nominally** expected from the mean of a range of identical instruments.
This specification is valid after the instrument has warmed up for 15 minutes (reference temperature 23°C ± 1°C).

3.1.1 Signatures

Measuring modes : with or without qualifier, repetitieve or single measurement with data-hold and 'latch unstable signature' mode
Display : 4 characters (0 to 9, ACFHPU)
Unstable indication : with '~' sign
Display refreshment : each 300 ms except for unstable signatures, which are shown immediately

INPUTS
- Data input : via data probe provided with 'hold' switch and indicators for hold mode and logic state
- Clock, Start, Stop and Qualifier : via POD
- Input impedance : data probe
  142 kΩ to logic 0 // 25 pF
  77 kΩ to 0,78 (dL + dH) V
  : POD
  100 kΩ to logic 0 // 25 pF
- V open data probe : mean value of dL and dH, between +9.2 and − 7.2 V
- Protection : 150 V continuously
  250 V for 10 seconds
  (max. peak 350 V)

3.1.2 Trigger Levels and Edges

Selection : TTL or VARiable

	TTL	VAR	
		default CMOS	setting range
Data low	<0.8 V	<1.5 V	independently adjustable
Data high	<2.0 V	<3.5 V	Between + and −
POD	1.4 V	2.5 V	12.7 V in 0.1 V steps

The default value for VARiable setting is for CMOS 5 V and is automatically set at switching on.
All levels can be shown in the display.
The trigger edges for clock start and stop and the low/high level of the qualifier can be selected and are indicated by LEDs.

3.1.3 Timing Data

Clock : maximum frequency 20 MHz
minimum pulse width 20 ns
Gate length : min. 1 clock cycle, max. no limit
Time between gates : min. 1 clock cycle

	Data probe	Start, Stop, Qualifier
Set-up time	10 ns	20 ns
Hold time	0	0

3.1.4 Logic State Indicator

Indicator : LED on data probe
bright for > dH
off for < dH
dim for > dL, <dH
Minimum detectable pulse width : 20 ns shown on LED for at least 100 ms
Trigger levels : as for signatures

3.1.5 Memory Modules (Option PM 9140/PM 9141)

This memory option enables the instrument to be adapted fore use with memory modules that provide direct comparison of measured signatures previously stored in a module. Any incorrect signature detected during measurement gives an error indication in the display and an audible alarm signal.

Storage capacity : trigger levels for probe and pod
separate trigger edges for normal and qualified mode
maximum of 125 signatures
Read time : 1 ms/signature
Loading : via PM 2544, using 'store' mode
Supply : Li battery (lifetime 5 years)

3.1.6 Peak Voltage Measurements

Input : via data probe
Measuring mode : highest or lowest peak
Range : −12.6 V to +12.6 V
Resolution : 0.1 V
Accuracy : ± 2% of reading ± 0.2 V
± 2% of peak to peak value
Minimum pulsewidth : 20 ns
Maximum repetition time : 50 ms

3.1.7 Frequency Measurements

Input : via data probe
Ranges : autoranging 100 kHz, 1 MHz, 10 MHz. and 20 MHz.
Minimum pulse width: 20 ns.
Resolution : 1 in 100,000 counts (1 Hz in 100 kHz range)
Gate time : 1 second
Trigger mode : positive edge, passing low and high threshold level
Trigger level : adjustable as for signatures
Accuracy : ± 0,01% of reading ± 1 count

3.1.8 Time Measurements

Input	: via POD: start and stop
Ranges	: autoranging 10 ms to 10^5s in eight ranges
Resolution	: 1 in 1000,000 counts (100 ns in 10 ms range)
Start and stop pulses edge	: selectable
Trigger level	: adjustable as for signatures
Minimum pulse width	: 100 ns
Accuracy	: 0.01% of reading ±2 counts

3.1.9 Event Counting

Input	: event via data probe start and stop via POD
Ranges	: 10^5 to 10^{11} in seven ranges, autoranging
Resolution	: 1 in 100,000
Trigger mode data	: positive edge, passing low and high threshold
Trigger level	: as for signature
Start and stop pulses	: as for time measurement
Accuracy	: at input frequency <10 MHz ±1 count >10 MHz ±2 counts

3.1.10 Multimeter

MEASURING QUANTITY	V_{DC}	V_{AC} AC-coupled RMS (crest factor 2)	I_{DC}	R
Ranges all auto-or manual ranging	1000 mV 10 V 100 V 1000 V (max. 450V)		100 mA 10 A	Range / Current 1000 Ω / 1 mA 10 kΩ / 100μA 100 kΩ / 10μA 1 MΩ / 1μA 10 MΩ / 100nA
Max resolution	100μV		10 μA	0.1Ω
Accuracy ± % reading ± digits	±0.2% ±5 d	±0.5% ±10 d (40 Hz 1 kHz) ±0.1% ±10 d (1 kHz 10 kHz) ±5% ±10 d (10 kHz 20 kHz)	±0.5% ±10 d	±0.5% ±10 d except MΩ range with ±1% ±10 d
Temperature coefficient ± % of reading /°C	±0.03%	±0.03%	±0.05%	±0.03% to 1 M ±0.05% in 10 M range
Input characteristics	up to 10 V 9.8 M Ω over 10 V 8.85 MΩ	up to 10 V 2 MΩ//50pF over 10 V 1.8 MΩ//50pF	voltage over input <200 mV	voltage at open input: 3 V
Common-mode (CM) Rejection	d.c 100 dB 50 Hz 100 dB	d.c 100 dB 50 Hz 80 dB		
Maximum CM voltage	250 $V_{a.c}$ or d.c		250 $V_{a.c}$ or d.c	250 $V_{a.c}$ or d.c.
Series mode rejection at 50 Hz	80 dB	—		
Response time - excluding ranging - including ranging	<0.8 s < 1 s	<1 s <5 s	<0.8 s	<0.8 s < 2 s
Overload protection	450 V r.m.s 630 Vp		100 mA range 250 V r.m.s 350 Vp Fuse 315 mAF 10 A range no protection	250 V r.m.s 350 Vp
Bleeper warnings	>450 V r.m.s. in	range 1000 V	>110 mA >11A	<100 counts in MAN ranging mode
Maximum relative reference reading (ZERO SET)	-31.000 +31.000	-20.000 +31.000	-31.000 +31.000	-20.000 +31.000

Display: 4½ digit
max. reading 11.000 for absolute measurements
20.000 or 31.000 for relative reference measurements
polarity, function, auto/manual and offset indication in display
Overload indicated by OL in display

3.2 SAFETY CHARACTERISTICS

This appartus has been designed and tested in accordance with Safety Class I requirements of IEC Publication 348 Safety Requirements for Electronic Measuring Apparatus. VDE0411 and has been supplied in a safe condition. This manual contains some informations and warnings which must be followed by the user to ensure operation and to retain the apparatus in a safe condition.

3.3 ENVIRONMENTAL CONDITIONS

The environmental data mentioned in this instruction manual are based on the results of the manufacturer's checking procedures.
Details on these procedures and failure criteria are supplied on request by the PHILIPS organisation in your country. or by N.V. PHILIPS' GLOEILAMPEN FABRIEKEN. SCIENTIFIC & INDUSTRIAL EQUIPMENT DIVISION. EINDHOVEN. THE NETHERLANDS.

3.3.1 Climatic Conditions

In accordance with Group 1 of IEC 359 with extension of the temperature limits.

Reference temperature	:	23°C ± 1°C
Rated range of use	:	0°C . . . 45°C
Limit range of storage and transport	:	−40°C . . . +70°C
Relative Humidity	:	20 . . . 80% non-condensing max. dew-point 25°C

3.3.2 Mechanical Requirements

In accordance with Group 2 of IEC 359.

3.4 INITIAL CHARACTERISTICS

Maximum dimensions

- Height	:	107 mm
- Width	:	225 mm
- Depth	:	305 mm
Maximum weight (mass)	:	2,8 kg
Cabinet material	:	ABS

3.5 MAINS SUPPLY CONDITIONS

In accordance with IEC 359, Group S2

Mains supply voltage	:	220 Vac (instrument can be adapted for 92 V, 110 V, 128 V, 202 V and 238 V. Refer to the Service Manual.
Rated range of use	:	± 10%
Mains supply frequency	:	50 Hz ± 1%
Rated range of use	:	48 Hz to 63 Hz
Power consumption	:	20 VA

3.6 ELECTROMAGNETIC INTERFERENCE

This instrument meets the requirements of CISPR-Publ. 11.

3.7 CALIBRATION

Calibration interval	:	6 months
Warm-up time before calibration	:	1 hour

4. ACCESSORIES

4.1 SUPPLIED WITH THE INSTRUMENT

Measuring leads with probes PM 9266.
Mains cable.
Data Probe with GROUND lead, spare probe tips and DIL test caps.
POD with START (green), STOP (red), CLOCK (yellow) and GROUND (black) lead.
Measuring clips for START, STOP, CLOCK and GROUND.
Accessory case
Spare fuses

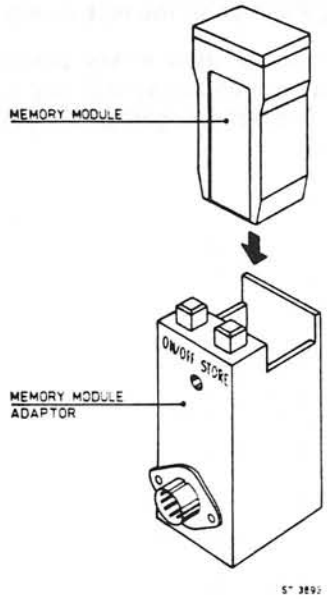
63 mA for 202V, 210V, 220V, 238V mains	SLOWBLOW
125 mA for 92V, 110V, 128V mains	SLOWBLOW
315 mA Multimeter input fuse	FAST
100 mA Multimeter power supply	SLOWBLOW
	(250V DIN 41571)

Operating manual

NOTE: All PHILIPS oscilloscope probe accessores can be used in combination with the data probe.
The data probe, POD and PM2544 are a unit
One of the elements should not be replaced without adjustment.
Refer to the Service Manual of the PM2544.

4.2 OPTIONALLY AVAILABLE

- 1 Memory module adaptor PM 9140/01 with 3 memory modules.
- 3 Memory modules PM 9141/01.



Memory Option

5. INSTALLATION INSTRUCTIONS

5.1 INITIAL INSPECTION

Check the contents of the shipment for completeness and note whether any damage has occurred during transport. If the contents are incomplete, or there is damage, a claim should be filed with the carrier immediately, and the Philips sales organisation should be notified in order to facilitate the repair or replacement of the instrument.

5.2 SAFETY INSTRUCTIONS

5.2.1 Earthing (Groundling)

Before any other connection is made the instrument shall be connected to a protective earth conductor in one of the following ways:

- via the three-core mains cable; the mains plug shall be inserted only into a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension cord without protective conductor.

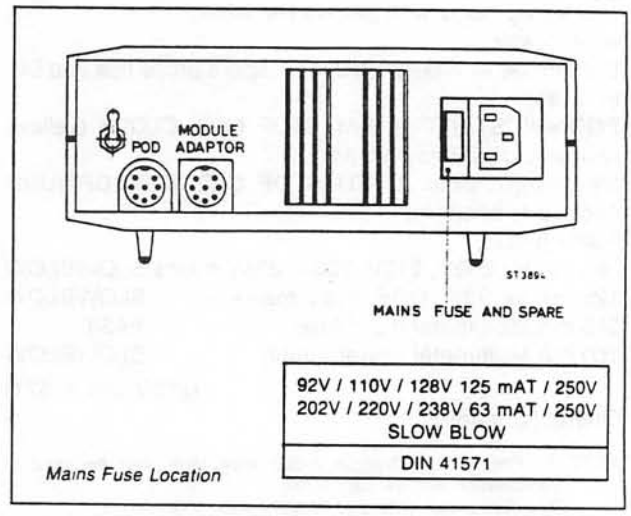
WARNING Any interruption of the protective conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous. Intentional interruption is prohibited.

5.2.2 Mains Voltage Setting and Mains fuse

- Before inserting the mains plug into the mains socket, make sure that the instrument is set to the local mains voltage.

NOTE: If the mains plug has to be adapted to the local situation, such adaption should be done by a qualified person only.

- The instrument shall be set to the local mains voltage only by a qualified person who is aware of the hazard involved.
  From the factory on the PM 2544 is set to a local mains voltage of 220 V. For modification to 92 V, 128 V, 202 V or 238 V refer to the service manual of this instrument.
- Make sure that only fuses of the required current rating, and of the specified type, are used for renewal. The use of repaired fuses, and/or the short-circuiting of fuse holders, are prohibited.
  The fuse is located in a holder on the rear panel, adjacent to the mains socket. To replace it, first remove the mains cable and prise out the lift-out lug with a screwdriver.'



Mains Fuse Location

The fuse shall be renewed only by a qualified person who is aware of the hazard involved.

WARNING The instrument shall be disconnected from all voltage sources when a fuse is to be renewed, or when the instrument is to be adapted to a different mains voltage.

5.2.3 Operating Position of the Instrument

The instrument may be used in any position. Do not position the instrument on any surface that produces or radiates heat, or in direct sunlight for long periods.

6. OPERATING INSTRUCTIONS

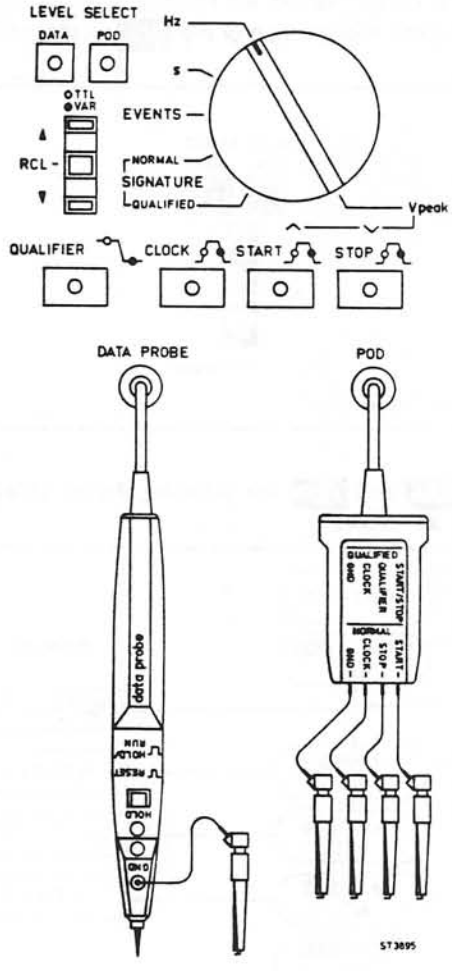
6.1 GENERAL INFORMATION

This section outlines the procedures and precautions necessary for operation. It identifies and breifly describes the functions of the front and rear panel controls and indicators, and explains the practical aspects of operation to enable an operator to evaluate quicly the instrument's main functions.

6.2 SWITCHING ON

After the instrument has been connected to the mains (line) voltage in accordance with clauses 5.2.1. and 5.2.2 it can be switched on.
Having switched on the instrument, it is immediately ready for use.
With normal installation, in accordance with Section 5 and after a warming-up time of 15 minutes, the characteristics specified in Section 3 are valid.

6.3 LOGIC METER FUNCTIONS



Logic Meter Controls

6.3.1 General Information

This section describes the functions of the PM 2544 that are referred to as logic functions, and are measured via the data probe and/or the pod.
Basically, these are the functions of voltage, current and resistance, require a data stream for measurement purposes.
These logic functions are selected by the left-hand positions of the function selection switch as shown.

6.3.1.1 Function selection summary

The following table summarizes the facilities available and functions that need to be selected to perform the various logic measurements.

FUNCTION	RANGES	DATA PROBE INPUT	POD INPUT
Hz	auto-ranging 100 kHz 1 MHz 10 MHz 100 MHz (max. 20 MHz)	DATA INPUT GND STATE LED	
s	auto-ranging 10 ms 100 ms 1000 ms 10 s 100 s 1000 s 10.000 s (min. 100 ns)		START STOP GND
EVENTS	auto-ranging 100.000 | 100.000 M	DATA INPUT GND STATE LED	START STOP GND
SIGNATURE (NORMAL)		DATA INPUT GND STATE LED HOLD/RUN -RESET SWITCH	START STOP CLOCK GND
(QUALIFIED)		DATA INPUT GND STATE LED HOLD/RUN -RESET SWITCH	START STOP QUAL. CLOCK GND
Vpeak	– 12.6 V up to + 12.6 V (maximum repetition time 50 ms) Modes: V top ^ V bottom v	DATA INPUT GND (ignore STATE LED)	

TRIGGER SELECTION - HZ, s, EVENTS, SIGNATURE
Trigger level selection of DATA and/or POD: - TTL (initial) - VARiable (default CMOS 5 V)
Trigger edge selection: - RISING or FALLING for START , STOP, CLOCK
Trigger level selection of QUALIFIER: -HIGH or LOW

6.3.1.2 Trigger level selection

To provide for measurements in a variety of logic circuits, appropriate trigger levels can be selected, as given in the following table.

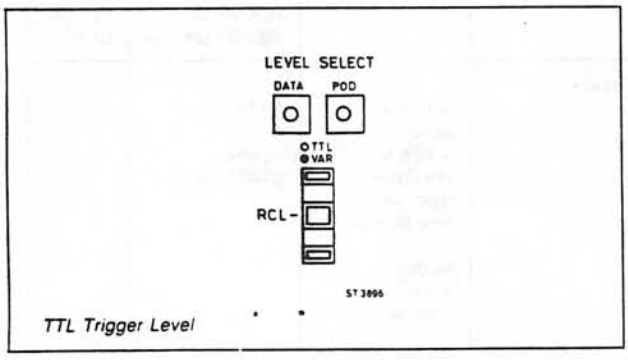
TRIGGER LEVEL TABLE	POWER ON	DATA and/ or POD	RCL ▲ ▼
	TTL	CMOS 5V	VARIABLE
DATA PROBE DL	+ 0.8V	+1.5V	- 12.7V + 12.7V
DH	+2.0V	+3.5V	
POD P	+1.4V	+2.5V	
	INITIAL	DEFAULT	

DL = LOW LEVEL DATA PROBE
DH = HIGH LEVEL DATA PROBE
P = LEVEL OF POD

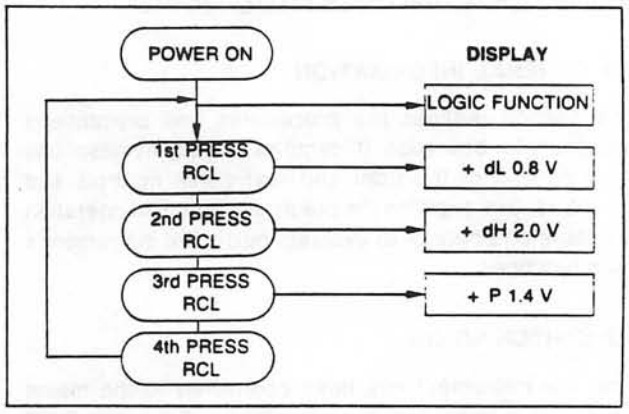
At initial switch-on of the PM 2544 TTL trigger levels are selected. CMOS 5V or variable trigger levels are obtain able by selecting DATA and/or POD. The default value for VARIABLE is CMOS 5V.
The state LED on the probe will indicate correct triggering if the input signal is measured with the data probe while adjusting the trigger level.

INITIAL TTL (DATA and/or POD)

The initial (TTL) values are obtained when switching on (POWER ON), but the logic function is displayed.
The TTL initial values are displayed by depressing the mid-position of the RCL (RECALL) pushbutton (available in all logic functions except Vpeak).



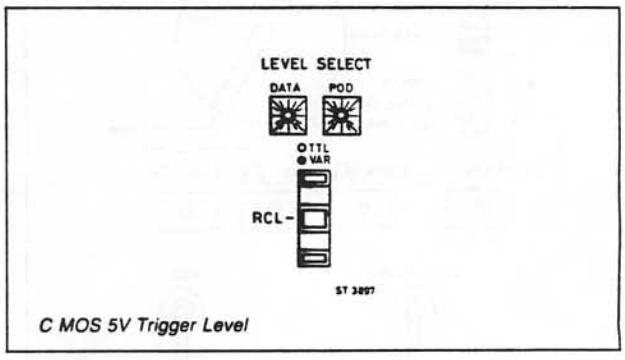
TTL Trigger Level



VARIABLE MODE (DATA and/or POD)

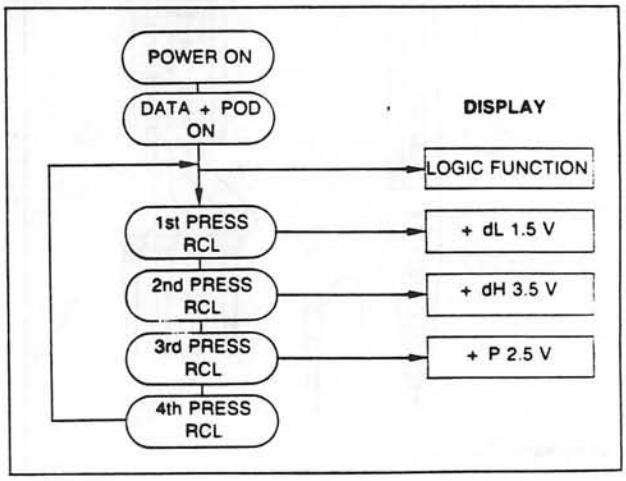
a) DEFAULT CMOS 5 V.

The default values are obtained in the logic functions (Hz, s, EVENTS, SIGNATURE) after switching on POWER ON and depressing the LEVEL SELECT DATA and/or POD pushbutton (logic function displayed).
If the DATA and/or POD pushbuttons are selected, the one not selected stays in the TTL mode and cannot be varied. The default values are recalled and displayed by depressing the mid-position of the RCL pushbutton.

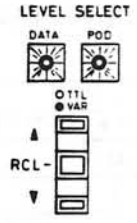


C MOS 5V Trigger Level

If both DATA and POD are selected, the variable-mode display is as follows.



b) VARIABLE LEVEL



Variable Trigger Level ST 3898

When the default data is displayed, by depressing the mid-position of the RCL pusbutton as shown above, this may be varied between – 12.7 V and + 12.7 V by means of the ▲ and ▼ ends of the RCL pushbutton.

To vary the default CMOS 5 V values, recall each one to the display in turn by depressing the mid-position of the RCL pushbutton.

For example:
With low level default data recalled by first press of RCL mid-position the display shows
+ dL 1.5 V.

This value of the data probe can be varied in a positive direction by ▲ or in a negative direction by ▼
A single depress varies by one digit.
Continuous depress gives automatic roll-over of digits, first slow and then fast after a short period.
To vary the other values, proceed in a similar way:

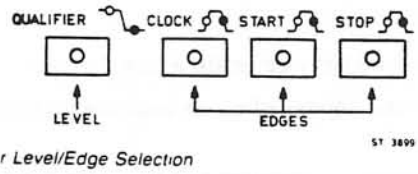
2nd press of RCL = + dH 3.5 V
Vary as required with ▲ ▼

3rd press of RCL = + P 2.5 V
Vary as required with ▲ ▼

4th press of RCL = display of logic function

6.3.1.3 Trigger edge/qualifier level selection

At switch-on, the four pushbutton LEDs are OFF, indicating high/rising selection for triggering the qualifier, clock, start and stop functions.
In the ON position, these LEDs indicate low/falling selection.
The START, STOP and CLOCK pushbuttons enable selection of either the rising **edge** for triggering, or the falling **edge** (LED ON).
The QUALIFIER pushbutton enables selection of either the **high level** or the **low level** (LED ON).



Trigger Level/Edge Selection ST 3899

Depending on the logic function, the trigger edge/qualifier level of relevant inputs can be selected.

FUNCTION	EDGE	INITIAL
S	START STOP	RISING
EVENTS	START STOP	
SIGNATURE NORMAL	START STOP CLOCK	
SIGNATURE QUALIFIED	START STOP CLOCK	
	QUALIFIER	HIGH

NOTE:
LEDs OFF = Rising Edge
High Level
LEDs ON = Falling Edge
Low Level
The new selected edges/levels in a function are automatically saved.

6.3.1.4 Data probe

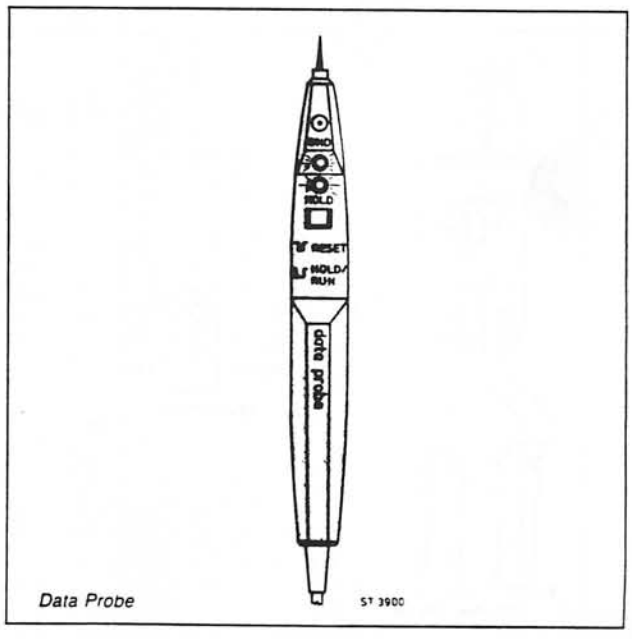
The connections, indicators and controls of the data probe are listed together with a brief explanation of their functions.

DATA : input for all logic function except seconds.

GND : ground of logic meter connected to ground of the pod (floating with respect to earth and ground of multimeter ⊥). For h.f. measurements connect ground of pod and probe together to ground of device under test always use as short possible ground leads.

STATE : state indication of the input signal.

The LED blinks at the frequency of the input signal up to 3 Hz. If input signal is higher than 3 Hz the blink frequency stays at 3 Hz.
STATE blinks of triggering takes place.
If STATE is not blinking while measuring, adjust your trigger level.



Data Probe ST 3900

HOLD : data hold indication in the signature function.

Follows the HOLD/RUN, RESET switch.
- End of measurment indicated by blinking in HOLD mode.

HOLD/RUN RESET : switch for HOLD/RUN, RESET in the signature function.
Normal (before depress) = RUN
1st depress for > 1 s = HOLD
2nd depress for < 1 s = RESET (1 measurement)
End of measurment indicated when LED blinks.
3rd depress for >1 s = RUN

NOTE: The data probe, POD and PM 2544 are a unit. One of the elements should not be replaced without adjustment. Refer the Service Manual of the PM 2544.

6.3.1.5 POD

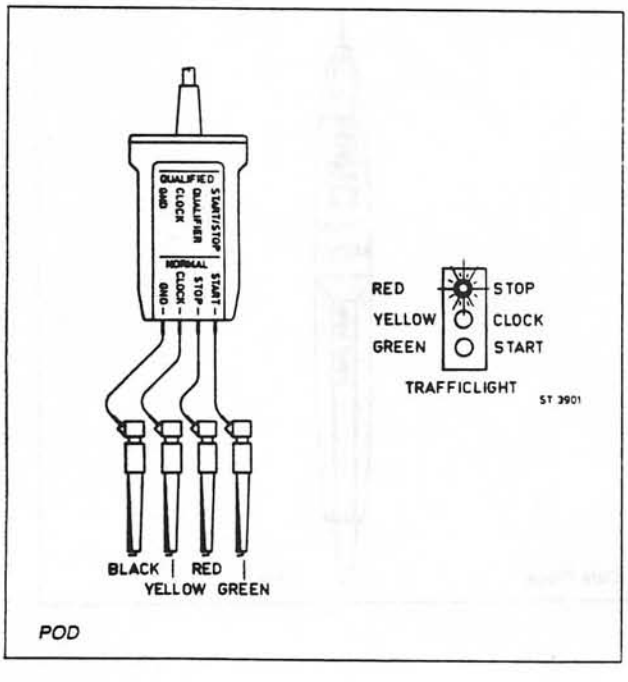
The connections of the POD are listed with a brief explanation of their functions.

GND : Ground of logic meter connected to ground of the probe (floating with respect to earth and ground of multimeter ⊥). For h.f. measurements connect ground of pod and probe together to ground in device under test. Always use as short as possible ground leads.

START - START/STOP : START; used in functions s, EVENTS, SIGNATURE NORMAL
START/STOP; combined input, used in QUALIFIED SIGNATURE mode.

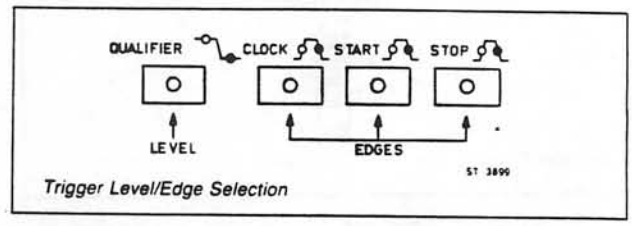
STOP - QUALIFIER : STOP; used in function s, EVENTS, SIGNATURE NORMAL
QUALIFIER: used in function QUALIFIED SIGNATURE

CLOCK : Clock input used in both signature functions.



POD

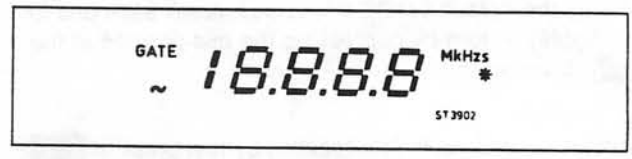
The colour-coded leads of the POD can be easely identified when connecting into logic circuits by use of a 'traffic-light' mnemonic.



Trigger Level/Edge Selection

START, STOP, CLOCK and QUALIFIER are related to the trigger edge/qualifier level selection pushbuttons.

6.3.1.6 Display



The display symbols of the PM 2544 are listed below with a brief explanation of their functions.

GATE : open gate time in functions Hz, s, EVENTS and SIGNATURES
Except in the HZ function, the gate time is controlled by the START and STOP on the POD.

~ : unstable signature sign.

1.X.X.X.X. : display with decimal point indication in functions Hz, s, EVENTS.

X X X X : display in the SIGNATURE functions.

E. X X X X (with bleeper) : negative stored or compared signature in memory module mode.

.X.X.X.X : recalled signature from the memory module.

M : Mega
k : kilo
} Hz and EVENTS functions.

s : seconds in time mode.
store in memory mode

Hz : Hertz in Hz function.

H : Hold mode in function signatures.

* : latch unstable signature mode.

MH : memory / hold mode.

6.3.1.7 Bleep signals

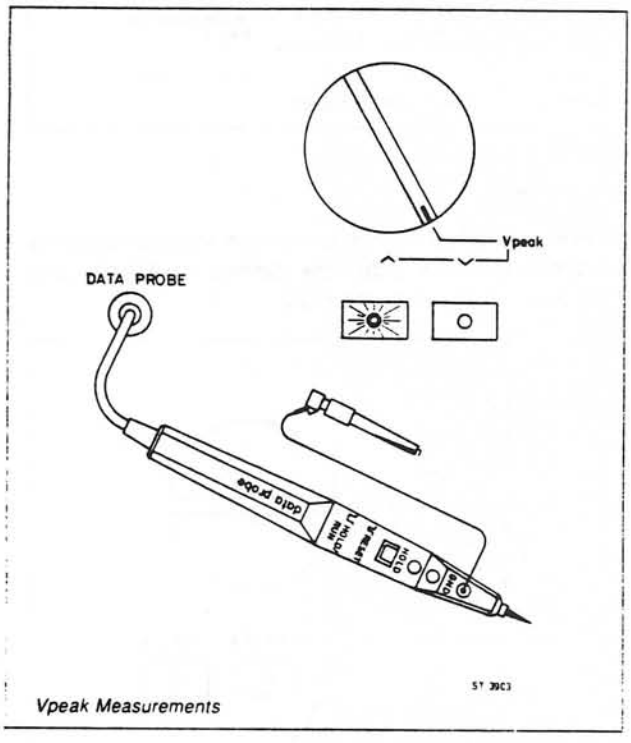
The following conditions generate a bleep signal:

- In latch unstable mode, when an unstable signature is captured (1 ×).
- In memory mode
  - When a signature is stored (1 ×).
  - When a positive signature is compared (1 ×).
  - When an negative signature is compared (2 ×).

6.3.2 MEASURING

The logic measuring functions of the PM 2544; namely, voltage peak, frequency, time, events and signature analysis measurements are each outlined in the following sub-sections.

6.3.2.1 Vpeak



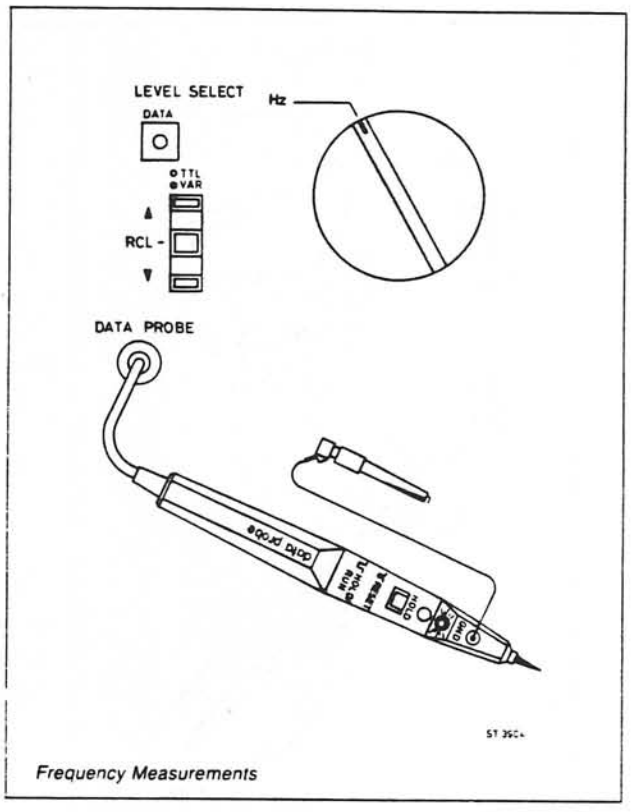
Vpeak Measurements

The Vpeak function permits the top ^ or bottom ˅ peak of a voltage waveform to be measured over a range from −12.6 V up to +12.6 V.

The top peak or the bottom peak mode can be selected by depressing either the ^ or ˅ pushbutton respectively. Initially, Vpeak ^(top) is selected.
The inputs signal must be measured with the data probe, with GND connected to the probe or pod.

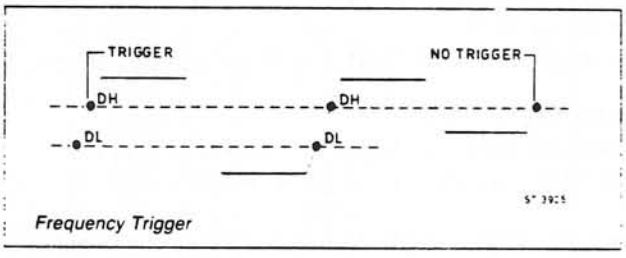
While measuring, the STATE led should be ignored.

6.3.2.2 Frequency (Hz)



Frequency Measurements

Frequency measurement (Hz) is an automatic function, giving:
- auto-ranging from 1 Hz up to 100 MHz
- auto-triggering on positive-crossings of DH trigger level after passing dL.



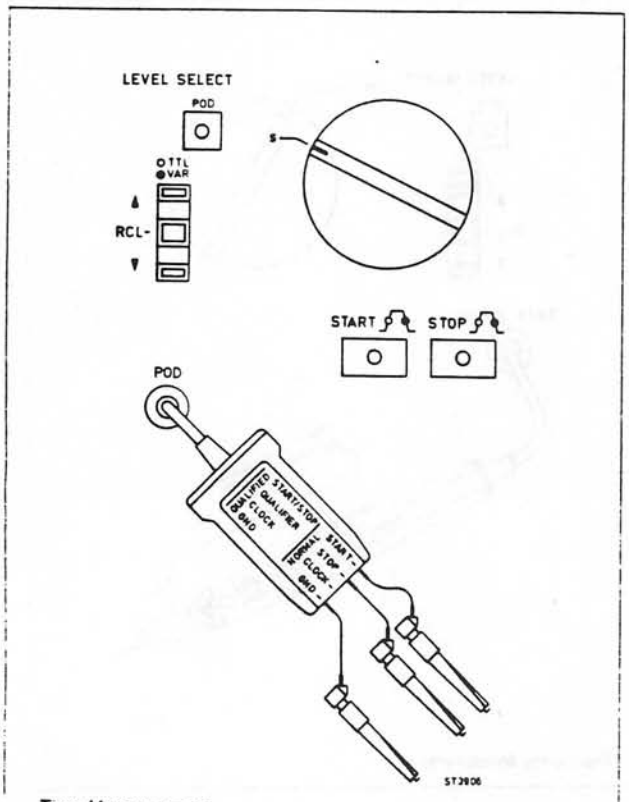
Frequency Trigger

The trigger level of the probe can be selected between
- initial TTL (dL = +0.8 V, dH = +2.0 V)
- VARiable (default CMOS 5 V) dL and dH selectable between −12.7 V and +12.7 V

Refer to Section 6.3.1.2 Trigger level selection.

The state of the input signal is indicated on the data probe 'STATE' LED:
- blinks at input frequencies below 3 Hz.
- blinks at 3 Hz for input frequencies ≥3 Hz.

6.3.2.3 Time(s)



Time Measurements

The time function is an automatic function giving:
- auto-ranging over a time period from 100 ns to 100,000 s.

The time, or gate open period is measured between a START and a STOP pulse derived from the circuit under test via the POD.
The trigger level of START and STOP can be selected from:
- initial TTL + 1.4 V
- VARiable (default CMOS 5 V) – 12.7 V to + 12.7 V.

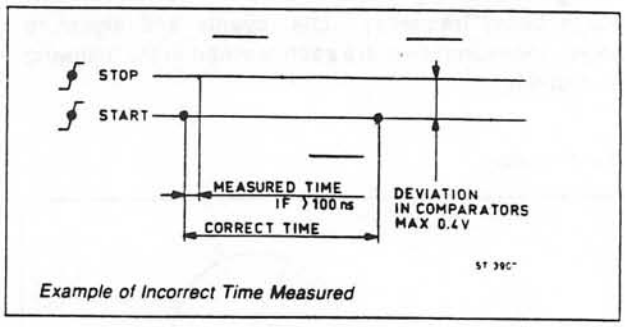
Refer to Section 6.3.1.2 Trigger level selection.

The trigger edge of the START and STOP can be selected to be either rising or falling.
Refer to Section 6.3.1.3 Trigger edge selection.
Initial values are:
- trigger level : TTL
- trigger edge : RISING

The PM2544 measures only via the POD in time(s) function.

NOTE: The new selected edges of START/STOP are saved when leaving the function.

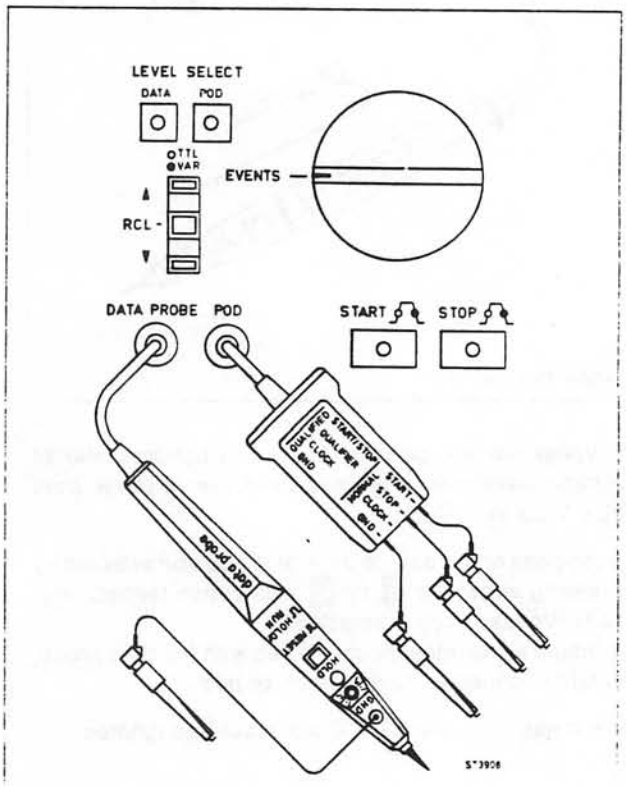
Due to separate comparators for START and STOP in the PM 2544 a difference in triggering may occur. This may cause incorrect time measurements especially with slow rising and falling edges.



Example of Incorrect Time Measured

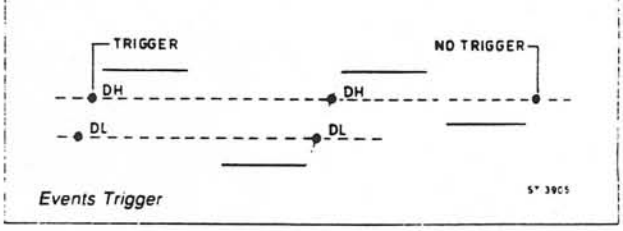
6.3.2.4 Events

The events function counts low to high transitions on the data probe during a gate time defined by START and STOP pulses applied to the POD.



Events Measurements

It is an automatic function with:
- auto-ranging fro 1 to 100,000 M counts (max. frequency 20 MHz)
- trigger occurs on positive-crossings of dH trigger level after passing dL.



Events Trigger

The trigger level of START and STOP and DATA PROBE can be selected from:
- initial TTL +1.4 V (POD)
  initial TTL dL +0.8 V; dH +2.0 V (PROBE)
- VARiable (default CMOS 5 V) −12.7 V to +12.7 V.

Refer Section 6.3.1.2 Trigger level section.
The trigger edge of the START and STOP can be selected to be either rising or falling.
Refer to Section 6.3.1.3 Trigger edge selection.
Initial vales are:
- trigger level: TTL
- trigger edge: RISING.

The STATE indication LED operates in the events function.

NOTE: The new selected edge of START/STOP are saved when leaving the function.

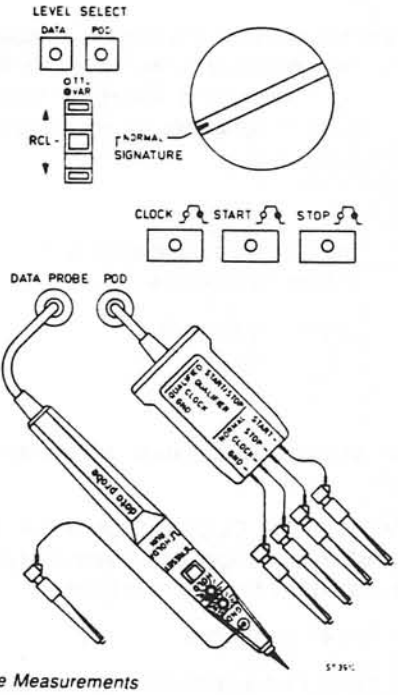
6.3.2.5 Signatures, normal and qualified

The signature, a 4-character word in hexadecimal code (0 - 9 ACFHPU), is captured in the free-run or hold mode from a data-flow signal on the probe under the control of the CLOCK, START, STOP and the QUALIFIER if required.

The two basic methods of taking signatures are:
- Normal Signature, using START, STOP, CLOCK, GND and DATA
- Qualified Signature, using combined START/STOP, QUALIFIER, CLOCK, GND and DATA.

The Latch Unstable Signature mode is an extra facility to the normal and qualified methods, selected by a toggle switch at the rear of the PM 2544. In this mode, the first unstable signature out of a stream of data can be captured.

Normal Signatures



Signature Measurements

START = Start measurement
STOP = Stop measurement
CLOCK = Clock in the state of the DATA signal and START, STOP

DISPLAY:

~ indicates unstable signature

H indicates HOLD mode

PROBE FACILITIES:

- STATE indication (LED)
- HOLD with switch (one depress >1 s) indicated by H in display and HOLD LED on probe
- One measurement possible in HOLD mode RESET for next (one depress <1 s)
- Escape from HOLD to RUN mode (one >1 s depress of HOLD switch)
- Trigger level of data input can be selected from:
  - initial TTL dL +0.8 V; dH +2.0 V
  - VARiable (default CMOS 5 V) −12.7 V to +12.7 V

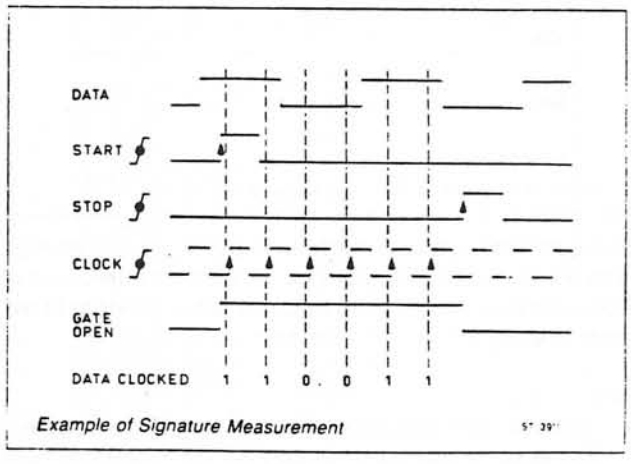
  Refer to Section 6.3.1.2 Trigger level selection.

POD FACILITIES:

- Trigger edge and trigger level of START, STOP and CLOCK can be selected as follows:
  - EDGE: rising or falling
    Refer to Section 6.3.1.3
    Trigger edge selection.
  - LEVEL: Initial TTL +1.4 V
    VARiable (default CMOS 5 V)
    −12.7 V to +12.7 V
    Refer to Section 6.3.1.2
    Trigger level selection.

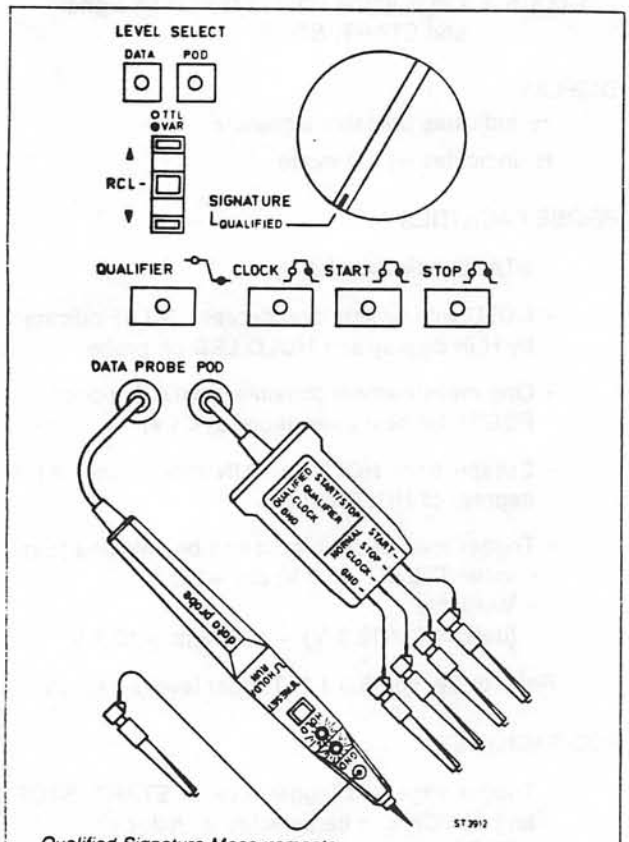
  Initial values are:
- trigger level: TTL
- trigger edges: RISING
- data probe: RUN mode

NOTE: The new selected edges of START, STOP and CLOCK are saved when leaving the function.



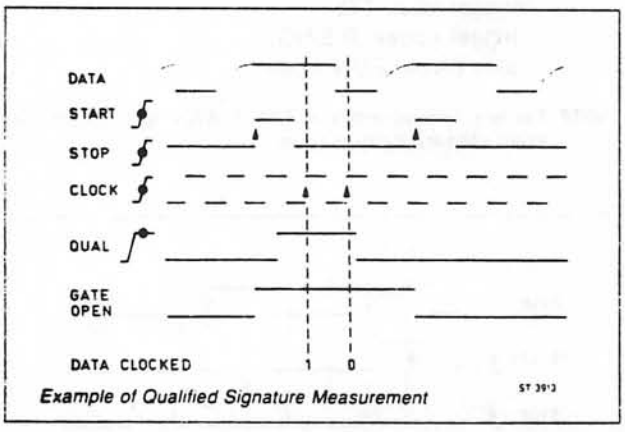
Example of Signature Measurement

Qualified Signatures



Qualified Signature Measurements

START = Start measurement
STOP = Stop measurement
CLOCK = Clock in state of START, STOP and of the DATA signal if QUALIFIER signal is true.
QUALIFIER = Enable data to be clocked in according to level selected HIGH or LOW



Example of Qualified Signature Measurement

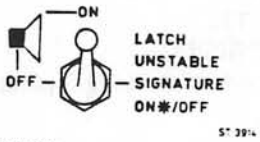
The qualified signatures function is identical to the normal signatures function except that an additional measuring condition (qualifier) is used to select either HIGH or LOW level to enable data to be clocked in.

Additional POD facilities:

The true level polarity of the qualifier can be selected in the same way as described for the START, STOP and CLOCK.

Initial values are:
- trigger level : TTL
- trigger edges/level: rising/high
- data probe : RUN mode

Latch Unstable Signature Mode



Latch Unstable Signatures

The facility to capture the first unstable signature from a stream can be used in either the NORMAL or QUALIFIED functions previously outlined. The operating details for measuring in this mode are as follows:

- The latch unstable signature mode is manually selected in the RUN mode, by means of a toggle switch on the rear of the M 2544.
- The ON condition is indicated by * on the display.
- When the first unstable signature that occurs in a stream is captured, the signature measurement is stopped and ~ is indicated on the display, together with a bleep warning.
- RESET for next measurement; i.e. until next unstable signature is received, is by a single depress of RESET pushbutton on probe.

6.3.3 Optional Memory Module for Signature Measuring

6.3.3.1 General

The memory option consists of a memory module adaptor that can be easily attached to the rear of the PM 2544 . It accepts plug-in memory modules for short-term or long-term storage of signatures for comparison testing.

Type numbers

PM 9140/01 : memory module adaptor with 3 memory modules

PM 9141/01 : 3 memory modules

Possibilities

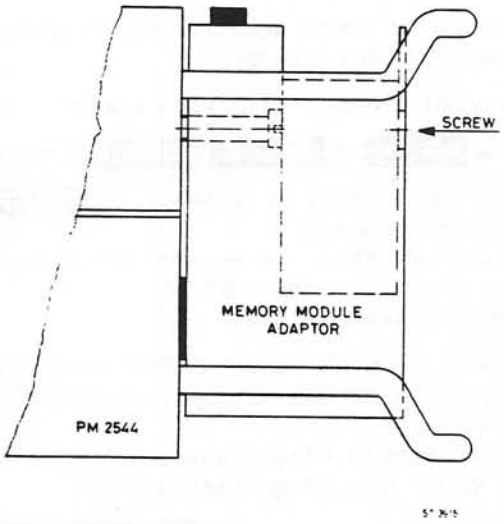
- capable of storing 125 different signatures (STORE pushbutton).
- saves START, STOP, CLOCK, QUALIFIER, POD and DATA PROBE trigger edges and levels after storing the first signature on the first memory location.
- recalls the stored signatures.
- compares the stored signatures with those measured and indicates errors
- provides write protection of the memery module.

Loading the memory

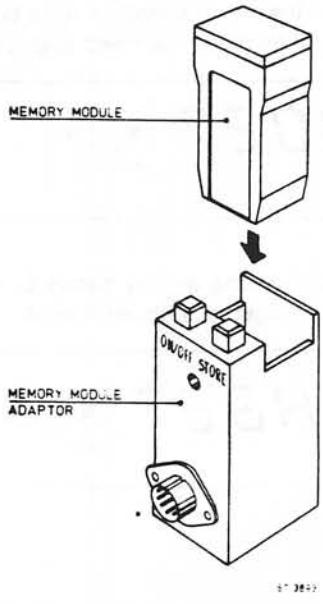
The memory is loaded by performing a measurement on a correctly functioning circuit under test. Afterwards, this loaded memory module can be used for testing identical circuit within the batch against signature comparisation. The RAM (Random-Access Memory) of the module is powered by a miniature battery to prevent loss of information at POWER OFF. The standby time of a module is 5 years.

Mounting the memory option

- Insert the 8-pole DIN plug of the memory adaptor in the corresponding DIN socket on the rear of the PM 2544.
- Fasten the screw.
- Plug a memory module into the adaptor.



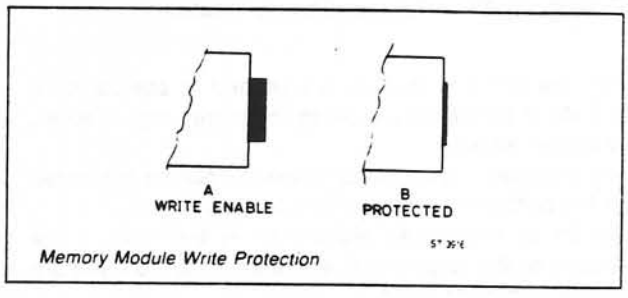
Mounting the Module Adaptor



Mounting the Memory Module

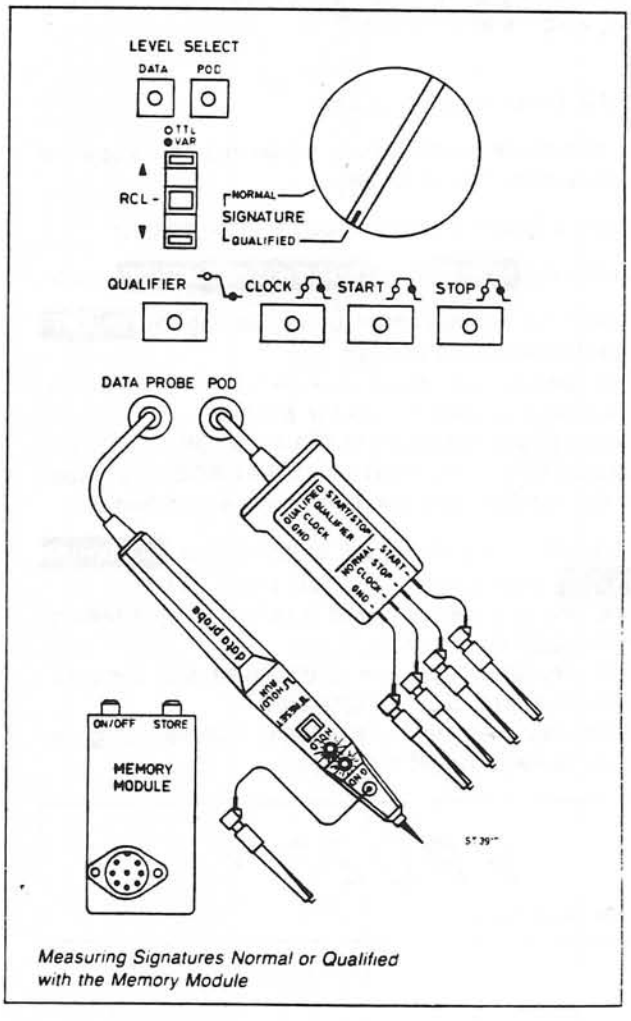
Write protection of the memory module

A jumper plug inserted at the top of the memory module protects the contents from being inadvertently overwritten. This jumper can be removed in the free-to-write (WRITE) position A, but in the PROTECTED position B it is turned through 180° and fully inserted.
For ease of identification, an appropriately labelled sticker can be fitted to each of the modules. These sticker is delivered with modules.



Memory Module Write Protection

6.3.3.2 Memory Module Facilities



Measuring Signatures Normal or Qualified with the Memory Module

The memory option permits 125 signatures to be stored manually.
If the memory module is switched on, automatically a test-byte is verified. If the battery voltage is too low the testbyte is destroyed and use of the module is not possible. In a new unloaded module first the testbyte also has to be stored.
The selected trigger edges of START, STOP, CLOCK and QUALIFIER level and the trigger level of the PROBE and POD and DATA PROBE are stored together with the signature stored in the first memory location.

When the memory module is switched to compare the PM 2544 is automatically set to the stored trigger levels and trigger edges.
The signatures of data being measured can be compared with the contents of the memory module.
Incorrect or non-stored signatures in the module are indicated on the display by E. and the measured signature together with two bleeps.

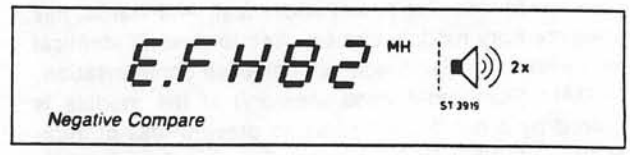
The signature 0000 is standardly regarded as an incorrect signature. Signature 0000 means node short-circuited to zero, which is an error condition.

6.3.3.3 Comparing Signatures

The procedure for comparing signatures on an optional memory module is as follows:

- Place a loaded memeory module in the adaptor.
- Select the NORMAL or QUALIFIED SIGNATURE mode.
- Select the memory mode by depressing the ON/OFF pushbutton on the adaptor.
  The display will show ————MH, M = Memory, H = Hold, if it does not refer to 6.3.3.5
  Stored edges and lelvels or START, STOP, CLOCK and QUALIFIER and the POD and DATA PROBE are loaded in the PM 2544 and the 'hold mode is switched on.
- Measure a signature by pressing the HOLD/RUN-RESET pushbutton on the data probe (<1 s).
  The end of a measurement is indicated by a blinking HOLD LED on the probe.
  The measured signature is displayed and compared with the stored bock of signatures.
  If the measured signature is found one bleep is given. (Can be switched-off at the rear).

If it is not found in the memory, the display shows E. and the measured signature together with two bleeps.



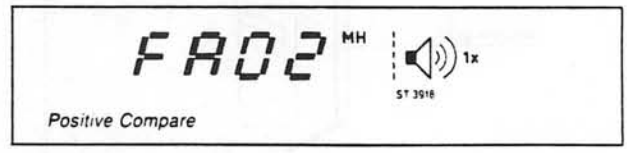
- Signature 0000 will always give an error indication.

NOTES: - When leaving the signature function or the hold mode the MEMORY MODE ON/OFF position is stored and re-loaded when re-entering the signature function.
- The loaded edges and levels can be altered manually in the MEMORY MODE. Reloading the stored memory values can simply be done by leaving and re-entering the memory mode via the ON/OFF pushbutton on the adaptor. (memory pointer is reset to location 1) or via another logic function (memory pointer stays on location).

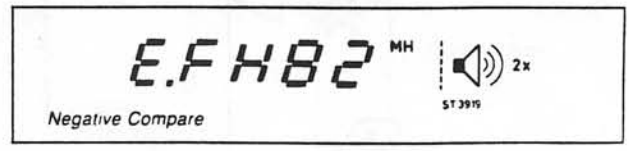
6.3.3.4 Storing a Block of Signature

The procedure for storing signatures on an optional memory mudule is as follows.

- Place a WRITE ENABLE module in the adaptor.
- Select the NORMAL or QUALIFIED SIGNATURE mode.
- Select the memory mode by depressing the ON/OFF pushbutton on the adaptor.
  The display will show ————MH (M = Memory, H = Hold). If it does not refer to 6.3.3.5.
  The TESTBYTE is verified now.
- Select the correct START, STOP, CLOCK and QUALI-FIER edges and levels and the trigger level of the POD and DATA PROBE.
  Refer to Section 6.3.1.1 Trigger level selection.
  Section 6.3.1.3 Trigger edge selection.
- Measure a signature by pressing the HOLD/RUN-RESET pushbutton on the data probe (< 1s).
  End of the measurment is indicated by a blinking HOLD led. The measured signature is displayed and compared with the contents of the memory module. if the signature already exists in the memory one bleep is given.

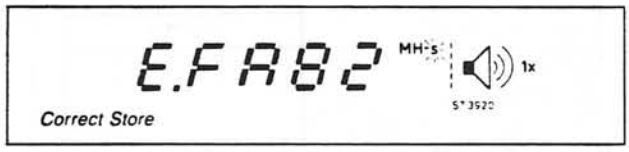


If it is a new signature, the display shows E. and the measured signature together with two bleeps.



This gives the possibility to check before storing whether a signature on a node is unique and whether the signature confirms to the repair information.

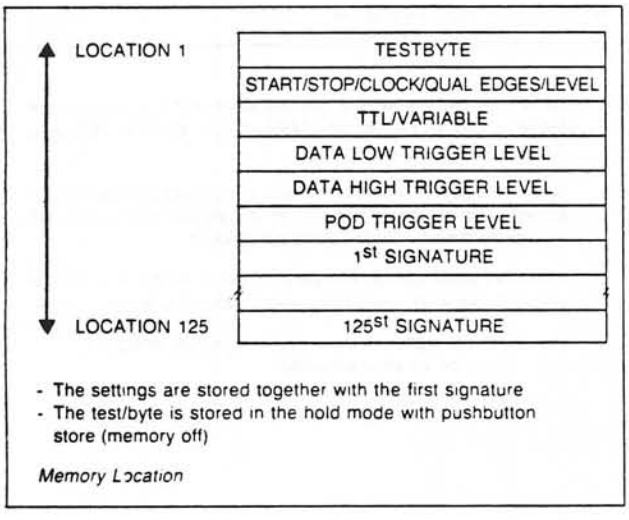
- Press the STORE pusbutton on the adaptor.
  The signature is stored on the first memory location, read back immediately and compared.
  If correct, a 's' appears on the display for 0.5 second and one bleep is given.
  In case of incorrect store the 's' is not shown but two bleeps is given.



Correct Store

When a signature is stored on the first memory location the selected edges and levels of START, STOP, CLOCK and QUALIFIER and the trigger levels of the POD and DATA PROBE are also stored.

Note the signature and the memory location in the memory location list.



- The settings are stored together with the first signature
- The test/byte is stored in the hold mode with pushbutton store (memory off)

Memory Location

- Measure the next signature.
- Press the STORE pushbutton again.
  The measured signature is stored in the next memory location and checked.
  The edges and levels are not stored again.
- Continue by measuring and storing up to the last signature required.
  Maximum number of signatures is 125.
  When the memory is full, the instrument does not react when the STORE pushbuttons pressed.
- A block of stored signatures should be terminated with the signature of logic 0 (0000).
  Signature 0000 is always seen as an incorrect signature.
  This signature signals the end of a stored block.
- Place the write protection in position PROTECTED.
  Refer to Section 6.3.3.1.
- If necessary use the sticker deliverd with the module to indicate what the contents repesent.
- It is advised to note down the memory location and the corresponding signatures in order to make modification of stored signatures easy.

NOTES: Remember that overwriting memory location 1 also restores the trigger edges and levels of START, STOP, CLOCK, POD and DATA PROBE.

Within a block of signatures the signature 0000 must not be stored. This is the terminator of a block of signatures. All signatures stored after this 0000 are ignored.

6.3.3.5 Resorting Testbyte

The procedure for restoring the testbyte is a follows.

If the MEMORY MODE cannot be entered by pressing the ON/OFF pushbutton on the adaptor the testbyte is incorrect.
This may be the case with a new unloaded module or if the battery in the module is flat.

The testbyte can be restored as follows:

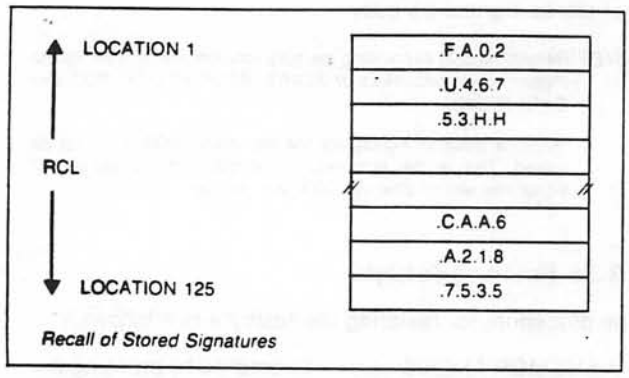
- Select the NORMAL or QUALIFIED SIGNATURE mode.
- Place the write protection in position WRITE ENABLE.
- Place the memory module in the adaptor.
- Select the HOLD mode with the HOLD/RUN pushbutton on the probe (press > 1 s).
  On the display a 'H' will appear.
- Press pushbutton STORE The testbyte is now loaded.
- Press pushbutton ON/OFF The measurements in the memory mode can now be made.

6.3.3.6 Recall Stored Signature

The procedure for reading stored signatures is as follows.

Stored signatures can be shown on the display.

- Place a memory unit in the memory adaptor.
- Select the NORMAL or QUALIFIED SIGNATURE mode.
- Select the memory mode with pusbutton ON/OFF on the adaptor.
  The display will show ————MH (M = Memory, H = Hold).
  If does not, refer to Section 6.3.3.5.
  Depress the top ▲ or ▼ bottom of the RCL pushbutton.
  With pushbutton ▲ the contents of memory location 1 is displayed. The ▼ pushbutton displays location 125.
  The four dots indicate the RECALL MEMORY MODE.
- Using the ▲ or ▼ of the RCL makes it possible to step through the 125 memory locations. The memory location is not indicated on the display.
  Only the signature is displayed.



Recall of Stored Signatures

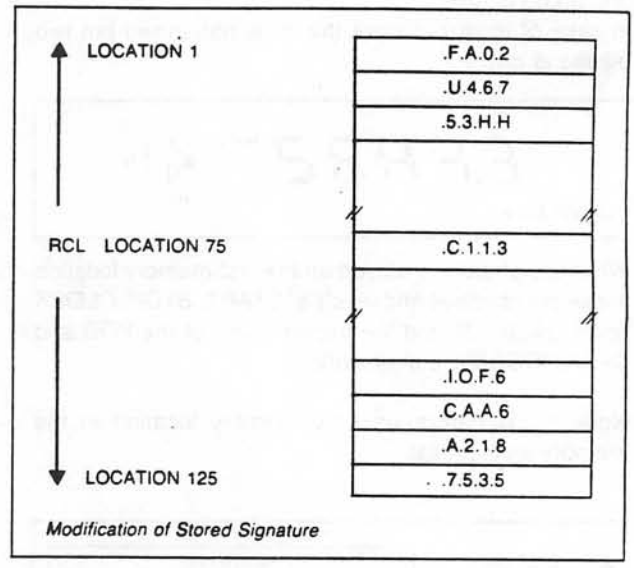
When storing signatures, a list should be made of the memory locations and the corresponding signaturs. This makes the recognising of the signatures easier.

- Recall of the normal measuring mode is made by depressing the RCL pushbutton.

6.3.3.7 Modifying a Stored Signature

The procedure for modifying a loaded signature is as follows:

- Place a WRITE ENABLE module in the adaptor.
- Search for the signature to be modified as described in Section 6.3.3.6.
- Recall the measuring function by depress of the RCL pushbutton.
- Measure the new signature to be stored by depressing the HOLD/RUN pusbutton on the probe (< 1s). Refer to Section 6.3.3.4.
- Press the STORE pushbutton on the adaptor. The new signature overwrites the signature on the selected memory location. Refer to Section 6.3.3.4.
- When continued with measuring and storing, the signatures are stored successively from this location on.
- After modifying, make the module PROTECTED again.



Modification of Stored Signature

NOTES: Remember that overwriting memory location 1 also restores the trigger edges and levels of START, STOP, CLOCK, POD and DATA PROBE.

Within a block of signatures the signature 0000 must not be stored. This is the terminator of a block of signatures. All signatures stored after this 0000 are ignored.

If a stored signature has to disappear out of the block, it may be useful to overwrite it with one switch is stored already.

Do not store a signature equal to the signature of logic 1. Logic 1 may be an error condition.

MEMORY MODULE LOCATION REFERENCE

No	Signature	Notes
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
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37		
38		
39		
40		
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		

No	Signatures	Notes
51		
52		
53		
54		
55		
56		
57		
58		
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64		
65		
66		
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86		
87		
88		
89		
90		
91		
92		
93		
94		
95		
96		
97		
98		
99		
100		

No	Signatures	Notes
101		
102		
103		
104		
105		
106		
107		
108		
109		
110		
111		
112		
113		
114		
115		
116		
117		
118		
119		
120		
121		
122		
123		
124		
125		

MODULE NO.:
INSTRUMENT:
DATE :
UP DATE :
UP DATE :

SETTING PM 2544

	NORMAL	QUAL
QUAL CLOCK START STOP		
DATA POD		

MEMORY MODULE LOCATION REFERENCE

No	Signature	Notes
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
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37		
38		
39		
40		
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		

No	Signatures	Notes
51		
52		
53		
54		
55		
56		
57		
58		
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64		
65		
66		
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90		
91		
92		
93		
94		
95		
96		
97		
98		
99		
100		

No	Signatures	Notes
101		
102		
103		
104		
105		
106		
107		
108		
109		
110		
111		
112		
113		
114		
115		
116		
117		
118		
119		
120		
121		
122		
123		
124		
125		

MODULE NO.:
INSTRUMENT:
DATE :
UP DATE :
UP DATE :

SETTING PM 2544

	NORMAL	QUAL
QUAL CLOCK START STOP		
DATA POD		

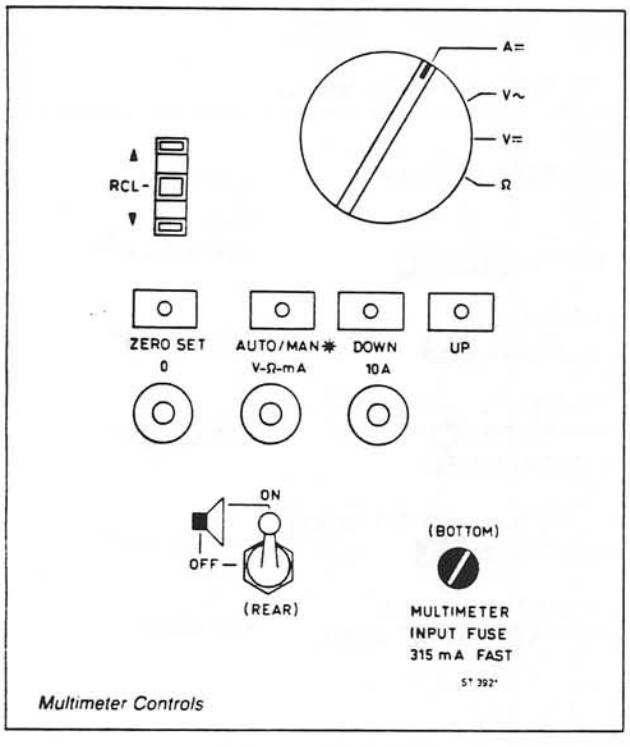
6.4 MULTIMETER FUNCTION

6.4.1 General information

This section describes the functions of the PM 2544 that are referred to as multimeter functions, namely, those that are measured via the two test leads connected to the front-panel sockets V-Ω-10mA, 10A and 0. These are the standard multimeter functions of voltage, current and resistance measurement.

These functions can be selected by the right-hand positions of the function selector switch as shown.

6.4.1.1 Function selection



Multimeter Controls

The following table summarizes the facilities and functions available in the multimeter part.

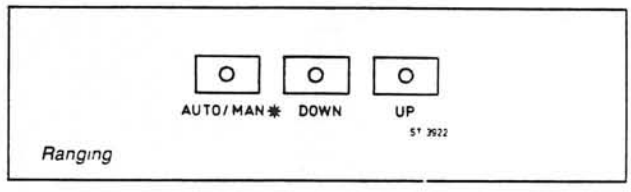
FUNCTION	RANGING	RANGES
A⎓	NONE	100 mA 10 A via separate 10 A socket
V~ /V⎓	MANUAL & AUTO	1000 mV 10 V 100 V 1000 V (450 V max.)
Ω	MANUAL & AUTO	1000 Ω 10 kΩ 100 kΩ 1000 kΩ 10 MΩ } continuity check with bleeper >100 digits

ZERO SET: It is possible to set a relative reference value in all functions.
The PM 2544 then displays the positive and negative deviations.

BLEEPER: Available in Ω function in manual range only, and can be switched off.
Permanently on in other functions (V⎓, V~, A⎓) at overload in the highest ranges.

6.4.1.2 Ranging

Manual or automatic ranging is available both for the voltage ranges and the resistance ranges.
Selection can be made by depressing the **AUTO/MAN ✱** pushbutton.
Manual ranging is indicated by an asterisk ✱ in the display.



Ranging

For MANUAL ✱

- Switch **AUTO/MAN ✱** to manual ranging mode (✱ in display).
- Change ranges as required with **UP** and **DOWN** pushbuttons.

Overload in any range is indicated by OL in the display (>10999).

For AUTOMATIC

- Switch **AUTO/MAN ✱** to automatic ranging (no asterisk displayed).

  Ranging is now performed automatically in the selected function.

- UP ranging at 10400
- DOWN ranging at 00896

6.4.1.3 Relative reference (ZERO SET)

In this mode, voltage, current and resistance measurements can be stored as reference values, successive measurements showing the deviation from the stored value.
Reference values can also be set manually by using the **RCL** **▲** **▼** control. These two methods of setting a relative reference, namely, by measuring a signal or by manual setting, are now outlined.

Measuring Relative Reference

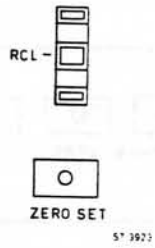
- Measure the input signal
- Depress the **ZERO SET** pushbutton
  The display will jump to zero and indicate: ZS (Zero Set). ✱ (Manual ranging)

The measured value is now the relative reference and subsequent measurements will display the deviation from this relative reference.

Recalling Relative Reference

- Depress mid position of the RCL pushbutton to RECALL relative reference value to the display, together with:
  Z (indicates relative reference value in display)
  ∗ (Manual ranging).
- The relative reference mode can be recalled by pressing the RCL pushbutton again.

Example of Measuring Relative Reference and Recall



Recall of Relative Reference

MEASURE REQUIRED RELATIVE REFERENCE	+01.500 V
PRESS ZERO SET	+00.000 v∗^{ZS}
MEASURE NEXT VALUE e.g. + 1.4900 V	−00.100 V∗^{ZS}
TO CHECK REL. REF. 1st PRESS RCL	+01.500 V∗^{Z}
TO RETURN TO R.R. MODE 2nd PRESS RCL	+00.100 V∗^{ZS}
TO LEAVE REL.REF. MODE PRESS ZERO SET AGAIN	+01.490 V

Leaving the Relative Reference mode also may be done with AUTO/MAN∗, UP, DOWN or FUNCTION switch.

Manual Setting the Relative Reference

- Depress the ZERO SET pushbutton
  The display will jump to zero and indicate: ZS (Zero Set) and ∗ (Manual ranging).

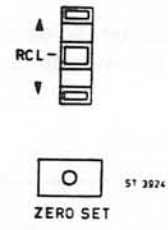
The value measured at this instant is now the relative reference value.

- Recall this value by depressing the midposition of the RCL pushbutton.

The display wil show this relative reference and indicate Z (relative reference in display) and ∗(Manual ranging).

- Press the top ▲ or bottom ▼ pushbutton to increase or decrease the relative reference value as required.
  On depress varies by one digit.
  Continues depress gives automatic roll-over (slow to fast action). Limits + or − 20000 and + or −31000.
- Return to relative reference mode via RCL
- To exit the ZERO SET mode, depress the ZERO SET pushbutton or the AUTO/MAN∗ UP DOWN or FUNCTION switch.

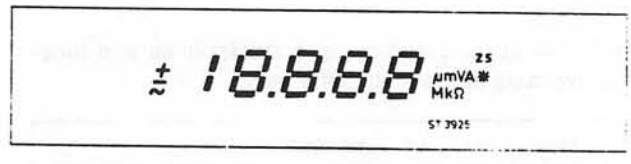
Example of Manual Setting (Relative Reference to + 02.500 V)



Manual Settings of Relative Reference

PRESENT DISPLAY	+01.450 V
TO CAPTURE: PRESS ZERO SET	−00.000 V∗^{ZS}
TO RECALL: 1st PRESS RCL	+01.450 V∗^{Z}
TO SET TO +2.5 V: PRESS TOP ▲ CONTINUOUSLY	+02.500 V∗^{Z}
TO RETURN TO R.R. MODE: 2nd PRESS RCL	+01.050 V∗^{ZS}
TO EXIT R.R. MODE: PRESS ZERO SET AGAIN	+01.450 V

6.4.1.4 Display



The display symbols of the PM 2544 relating to the multimeter functions are listed below with a brief explanation of their meaning.

±	:	polarity indication in functions V⎓ and A⎓ and Relative Reference mode (zero set).
~	:	alternating sign in function V~
ZS	:	ZERO SET indication in relative reference mode
Z	:	recall relative reference mode. The relative reference value can be modified with the RCL pushbutton.

* : MANUAL ranging indication

umVA
MkΩ : unit indications

1 8.8.8 8 : measured value with decimal points.

6.4.1.5 Bleep signals

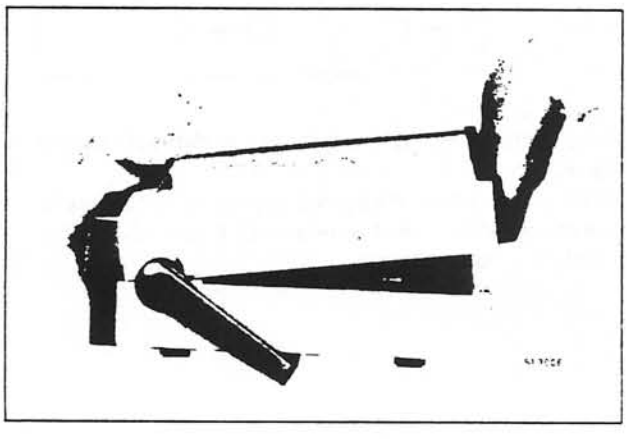
The following conditions generate a bleep signal.

V⎓ >450 V in 1000 V range
V~ >450 V in 1000 V range
mA⎓ >110mA
A⎓ >11A
Ω < 100 digits in manual ranging mode.
Switchable at the rear of the PM 2544.

6.4.1.6 Fuse Protection

The multimeter input is protected with a 315 mA FAST 250 V DIN 41571 Fuse.
The Fuse is located in the bottom cover of the PM 2544.

The power supply of the multimeter is protected with a 100 mAT slow blow 250 V DIN 41571 Fuse.
The fuse is located inside the PM 2544 on the transformer pcb.



For replace, remove the topcover as follows:

- Place the handle in its bottom position
- Remove the fixing screws after the rear which attach the topcover to the bottom cover and the rear.
- Lever the topcover and pull it backwards.

Make sure that only fuses of the required current rating, and of the specified type, are used for renewal. the use of repaired fuses, and/or the short-circuiting of fuse holders, are prohibited.

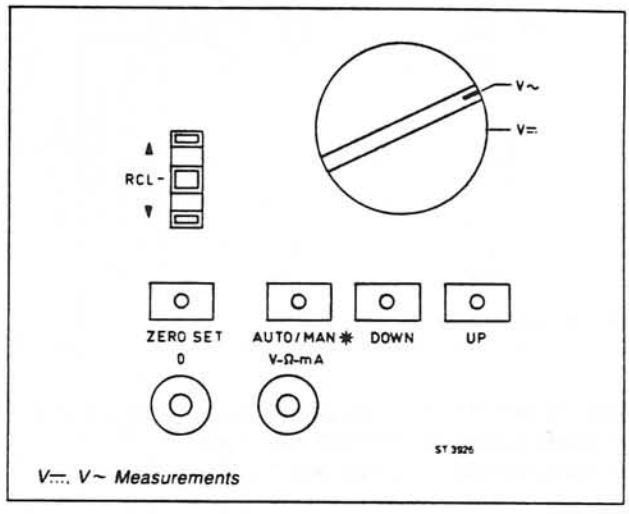
The fuse shall be renewed only by a qualified person who is aware of the hazard involved.

WARNING The instrument shall be disconnected from all voltage sources when a fuse is to be renewed, or when the instrument is to be adapted to a different mains voltage

6.4.2 MEASURING

The multimeter measuring functions of the PM 2544; namely, d.c. and a.c. voltages, d.c. currents, resistances including diode and continuity checks are described in the following sub-sections.

6.4.2.1 Voltages (V⎓ / V~)



V⎓, V~ Measurements

Measured with the test leads connected to V-Ω-mA and 0 front-panel sockets.

Ranges: 1000 mV
10 V
100 V
1000 V

Manual and auto-ranging facility (refer to Section 6.4.1.2 Ranging).

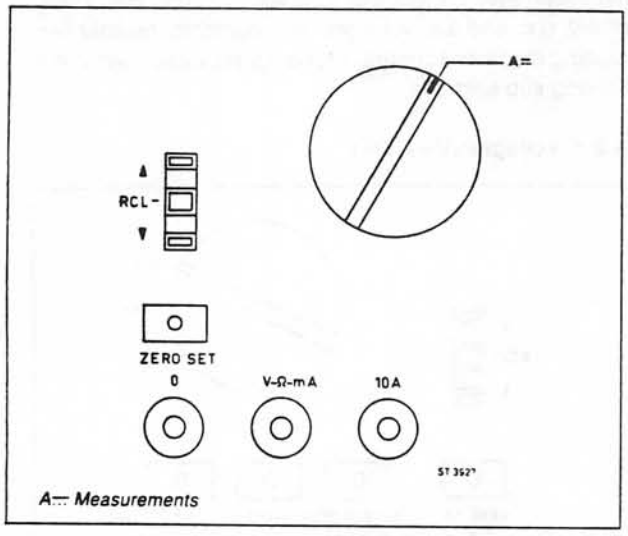
When the relative reference mode **ZERO SET** is required, refer to Section 6.4.1.3.

Maximum input voltages are:
450 V a.c. or d.c.
630 V peak

In the 1000 v range, overload OL is indicated >1099.9 V however, the maximum input voltage is 450 V.
A bleeper indication of overload is also given at input voltages of >450 V. (No switch-off).

The maximum input frequency in the V~rms function is 20 kHz (specified accuracy). Maximum common mode voltage: 250V ac or dc, 350 V peak.

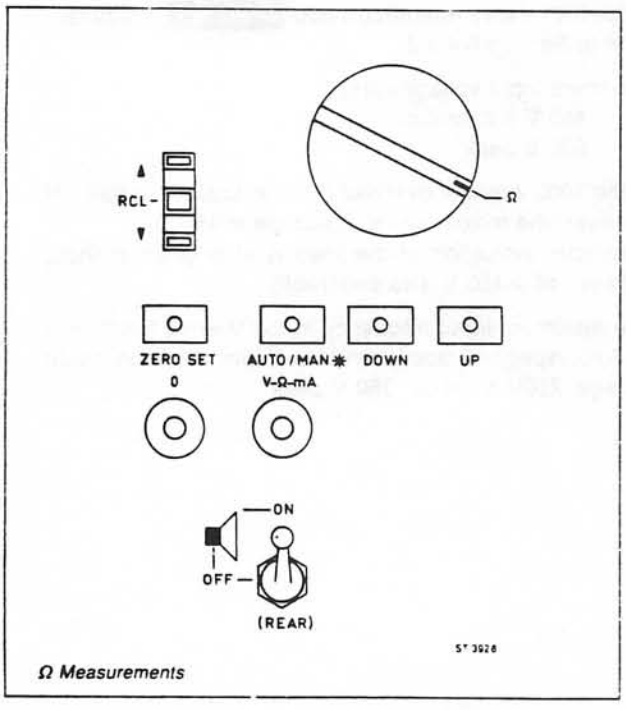
6.4.2.2 Currents (A⎓)



A⎓ Measurements

Measured with the test leads connected to V-Ω-mA and 0 front-panel sockets for the 100 mA range.
Test leads connected to 10A and 0 sockets for the 10 A range.
When the relative reference mode ZERO SET is required, refer to Section 6.4.1.3.
Protection: 100 mA with 315 mA Fuse
10 A no protection
Maximum common mode voltage, 250Vac or dc, 350Vpeak
OL indication and bleeper when 110 mA or 11 A reached.

6.4.2.3 Resistance (Ω) including diode and continuity checks.



Ω Measurements

Measured with the test leads connected to V-Ω-mA and 0 front panel sockets.

Ranges	CURRENT
1000 Ω	1 mA
10 kΩ	100 µA
100 kΩ	10 µA
1000 kΩ	1 µA
10 MΩ	100 nA

Manual and automatic ranging facility (refer to Section 6.4.1.2 Ranging).
When the relative reference mode ZERO SET is required, refer to Section 6.4.1.3.
Maximum common mode voltage 250 Vac or dc, 350 Vpeak.

Diode Checks
The 1000 Ω, 1 mA range is suitable for diode measurements (in manual ranging mode ✱).

DIODE TYPE	READING	
	Forward	Reverse
Silicon	06000 - 09000Ω	OL
Germanium	01000 - 03000Ω	OL
	0 V-Ω-mA + −	0 V-Ω-mA + −

Continuity Checks
Continuity check facility in all ranges in manual ranging mode ✱.
Bleeper signal when measured signal is <100 digits (value changeable in relative reference mode). Bleeper is optional (rear-panel switch).

7. FIRST AID SERVICING

Since this logimultimeter is designed and assembled with utmost care, the risk of breakdowns is small. If a breakdown should occur, it is at all times possible to contact the nearest Philips Service Organisation.
In case of simple breakdowns or users errors, however, and to avoid any loss of time and money, the user may try to locate the defective part or incorrect settins and carry out the repair or solution with the aid of the list given below.

Before proceeding to troubleshooting, make sure that the instrument is connected to the correct mains voltages and that this voltage is indeed supplied to the PM2544.

NO DISPLAY
- Check mains fuse.
- Check mains cord.

RUBBISH ON DISPLAY
- Switch off and on the PM2544.

NO FREQUENCY RESULT ON DISPLAY
- Check DATA PROBE trigger level.

The STATE led should be linking if correct triggered.

NO TIME RESULT ON DISPLAY (— — — —)
- Check the START and STOP trigger edges.
- Check the POD trigger level.

The GATE indication on the display should be blinking if correct triggered.
- Check connections in device under test.

NO EVENTS DISPLAY (— — — —)
- Check the DATA PROBE trigger level.

The STATE led should be blinking if correct triggered.
- Check the START and STOP trigger edges.
- Check the POD trigger level.

The GATE indication on the display should be blinking if correct triggered.
- Check connections in device under test.

NO SIGNATURE RESULT DISPLAY (— — — —)
- Check the DATA PROBE trigger level.

The STATE led should be blinking if correct triggered.
- Check the START, STOP, CLOCK and/or QUALIFIER trigger edges/level.
- Check the POD trigger level.

The GATE indication on the display should be blinking if correct triggered.
- Check connections in device under test.

NO VPEAK REASULT DISPLAY
- Check if the correct Vpeak mode is selected.

NO MULTIMETER RESULT DISPLAY
- Check the multimeter input fuse in bottom cover.
- Check power supply fuse inside the PM2544.

NO MEMORY MODULE RESULT DISPLAY
- Check if memory mode can be switched on.

If not; restore testbyte, replace battery
- Check write protection of the module
- Refer to section no signature result display

BLANK

Table 1-1. 5005A Specifications

SIGNATURE

Display: 4 digits. Characters 0-9, ACFHPU.
Fault detection accuracy: 100% probability of detecting single-bit errors; 99.998% probability of detecting multiple-bit errors.
Minimum gate length: 1 clock cycle (1 data bit) between START and STOP.
Maximum gate length: no limit.
Minimum timing between gates: 1 clock cycle between STOP and START.
Data probe timing:
Setup time: 10 ns (data to be valid at least 10 ns before selected clock edge.)
Hold time: 0 ns (data to be held until occurrence of selected clock edge.)
START, STOP, QUAL timing:
Setup time: 20 ns (signals to be valid at least 20 ns before selected clock edge.)
Hold time: 0 ns (signals to be held until occurrence of selected clock edge.)
CLOCK timing:
Maximum clock frequency: 20 MHz.
Minimum pulse width: 15 ns in high or low state.

Supplemental characteristics
Front panel indicators: flashing GATE light indicates detection of valid START, STOP, CLOCK conditions. Flashing UNSTABLE light indicates a difference between 2 successive signatures, and possible intermittent faults. Edge select lights indicate active edges for START, STOP, CLOCK and QUAL inputs.
Qualify mode: allows clock data qualification by an external signal.
DATA probe input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 10 pF.
START, STOP, CLOCK, QUAL input impedance: 100 kΩ; 10 pF.

FREQUENCY

Display: 5 digits.
Ranges: 100 kHz, 1 MHz, 10 MHz, 50 MHz, autoranged.
Resolution: 1 LSD (1 Hz on 100 kHz range).
Accuracy: ±0.01% of reading ±1 count.

Supplemental characteristics
Minimum pulse width: 10 ns in high or low state.
Gate time: 1 s, fixed.
Input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 10 pF.

TOTALIZING

Display: 5 digits.
Range: 0-99,999 counts.
Resolution: 1 count.
Accuracy: ±1 count.

Supplemental characteristics
Maximum input frequency: 50 MHz, with a minimum pulse width of 10 ns, and minimum pulse separation of 10 ns.
Minimum START/STOP pulse width: 20 ns.
DATA input impedance: 50 kΩ to the average value of "0" and "1" threshold settings (±6V max); 10 pF.
START, STOP input impedance: 100 kΩ; 10 pF.

TIME INTERVAL

Display: 5 digits.
Ranges: 10 ms, 100 ms, 1 s, 10 s, 100 s, autoranged.
Resolution: 1 count (100 ns on 10 ms range).
Accuracy: ±0.01% of reading ±1 count.

Supplemental characteristics
Minimum START/STOP pulse width: 20 ns.
START, STOP input impedance: 100 kΩ; 10 pF.

RESISTANCE

Display: 4 or 5 digits, depending on range.
Ranges: 30 kΩ, 300 kΩ, 1 MΩ, 3 MΩ, 10 MΩ, autoranged.
Accuracy: (at 15°C-30°C).

RANGE	FULL SCALE	ACCURACY	DISPLAY RESOLUTION
30 kΩ	29.999 kΩ	±1% of reading ±2 Ω	1 Ω
300 kΩ	299.99 kΩ	±1% of reading	10 Ω
1 MΩ	999.9 kΩ	±1% of reading	100 Ω
3 MΩ	2999. kΩ	±10% of reading	1 kΩ
10 MΩ	10000. kΩ	±10% of reading	10 kΩ

Supplemental characteristics
Input impedance: 20 kΩ to +2V.
Resolution: Actual measurement resolution, at higher values of resistance (>10 kΩ), is a multiple of the display resolution listed above, but is always well within the specified accuracy.

Table 1-1. 5005A Specifications (Continued)

DC VOLTAGE

Display: 4½ digits.
Ranges: ±25V, ±250V, autoranged; referenced to earth ground.
Accuracy: (at 15°C-30°C).

RANGE	ACCURACY	RESOLUTION
25V	±0.1 % of reading ± 2mV	1mV
250V (<100V)	±0.25% of reading ±20mV	10mV
250V (≥100V)	±0.25% of reading ±20mV	100mV

Supplemental characteristics
Input impedance: 10 MΩ

DIFFERENTIAL VOLTAGE

Reading: Reads input voltage present at the probe and displays difference between it and voltage at the time ΔV key was depressed.
Specifications: Same as for DCV, above. Voltage range is determined by larger of 2 compared voltages. Accuracy is valid for 1 minute after ΔV key depression.

Supplemental characteristics
Same as for DCV, above.

PEAK VOLTAGE

Display: 3½ digits.
Range: 0 – ±12Vp.
Resolution: 50mV.
Accuracy: ±2% of reading ±5% of p-p signal ±100mV.

Supplemental characteristics
Minimum peak duration: 10 ns.
Maximum time between peaks: 50 ms.
Input impedance: 100 kΩ; 10 pF.

LOGIC THRESHOLDS

Preset thresholds: (All levels ±0.2V).

FAMILY	DATA "1"	DATA "0"	CLOCK-ST-SP-QL
TTL	2.0V	0.8V	1.4V
ECL	-1.1V	-1.5V	-1.3V
CMOS	3.5V	1.5V	2.5V

Adjustable thresholds: Each preset threshold can be adjusted.
Range: ±12.5V, in 50mV steps.
Accuracy: ±2% of setting, ±.2V.

Operating characteristics
Logic threshold circuitry is operative during NORM, QUAL, kHz, TOTLZ and ms measurements.

GENERAL

Data probe tip: Acts as high-speed logic probe in the NORM, QUAL, kHz and TOTLZ modes. Lamp indicates high, low, bad-level and pulsing states. Minimum detected pulse width is 10 ns.
Data probe protection:
Continuous overload:
DCV, ΔV, kΩ modes only: ±250V AC/DC.
All other modes: ±150V AC/DC, 20V rms at input frequencies > 2 MHz.
Intermittent overload: ±250V AC/DC, up to 1 min, for all modes.
Timing pod protection:
Continuous overload: ±100V AC/DC, 20V rms at input frequencies > 2 MHz.
Intermittent overload: ±140V AC/DC, up to 1 min.
Auxiliary power supply: Three rear-panel connectors supply 5V at 0.7A total for pulser, current tracer or microprocessor exerciser.
Operating temperature: 0°C to +55°C.
Operating humidity: 95% RH at +40°C, except as specified otherwise for DCV, ΔV and kΩ modes.
Power: Selectable 100V, 120V, 220V or 240V AC line (+5%-10%), 48-440 Hz. 35 VA maximum.
Weight: Net: 3.5 kg, 8.0 lbs. Shipping: 10 kg, 22.5 lbs.
Size: 90 mm high × 215 mm wide × 410 mm deep (3½ in × 8½ in × 16 in), excluding handle.

*Specifications describe the instrument's warranted performance. *Supplemental characteristics* (shown in italics) are intended to provide information useful in applying the instrument, but are non-warranted performance parameters.

1-7. DESCRIPTION

1-8. The 5005A Signature Multimeter is a multipurpose instrument for troubleshooting electronic logic circuits to the component level. The 5005A can display digital "signatures" of logic circuits. This method of troubleshooting is called "signature analysis". Typically a logic product designed for signature analysis troubleshooting will have a programmed controller and a stored or externally-provided test program which can exercise most of the unit.

1-9. The 5005A also measures frequency, pulse counts, time intervals, DC voltages, voltage differences, positive or negative peak voltages, and resistances.

1-10. ACCESSORIES SUPPLIED

1-11. The accessories supplied with the 5005A are shown in *Figure 1-1*. Their description and part number are given below:

a. Depending on the customer's country, the line power cable supplied has one of six appropriate line (mains) connectors. Refer to *Figure 2-2*, Power Cable HP Part Numbers Versus Mains Plugs Available, for the part number of the correct cable.

b. Five detachable "grabber" test connectors are supplied with the 5005A. Their part number is 10230-62101. Refer to Section III for a description and use.

c. One ground lead for the data probe is supplied with the 5005A. Its part number is 05005-60116. One data probe tip cover is supplied. Its part number is 00547-40005.

1-12. INSTRUMENT AND MANUAL IDENTIFICATION

1-13. The instrument serial number is located just below the power input module on the rear panel. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The suffix however, is assigned sequentially and is different for each instrument. The contents of this manual applies to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-14. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-15. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-16. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

NOTE

Two manuals describe the 5005A. The OPERATING MANUAL has only the first four sections. (Keep it with the 5005A.) The OPERATING AND SERVICE MANUAL has all eight sections. (Keep it in your calibration/repair department.)

SECTION III
OPERATION

3-1. INTRODUCTION

3-2. This section gives complete operating information for the 5005A Signature Multimeter. Descriptions of all front panel controls, connectors, and indicators as well as an operator's check, operating instructions, and operator's maintenance are given.

3-3. The 5005A performs the analog measurements; DC volts (DCV), difference volts (ΔV), positive peak volts (Vp+), negative peak volts (Vp–), and resistance (kΩ), and digital measurements; Signature Analysis (NORM or QUAL), frequency (kHz), totalize (TOTLZ), and time interval (ms). In all digital measurements, selectable logic thresholds define the logic states for the incoming signals. All the measurements except Signature Analysis (NORM, QUAL) are standard measurements and require little explanation. However, Signature Analysis is a new concept and therefore is described in paragraph 3-16.

3-4. FRONT PANEL STORAGE COVER AND CABLE STORAGE

3-5. *Figure 3-1* shows the front panel storage cover with the handle locked in place for carrying. The line power cable is stored on the rear of the 5005A.

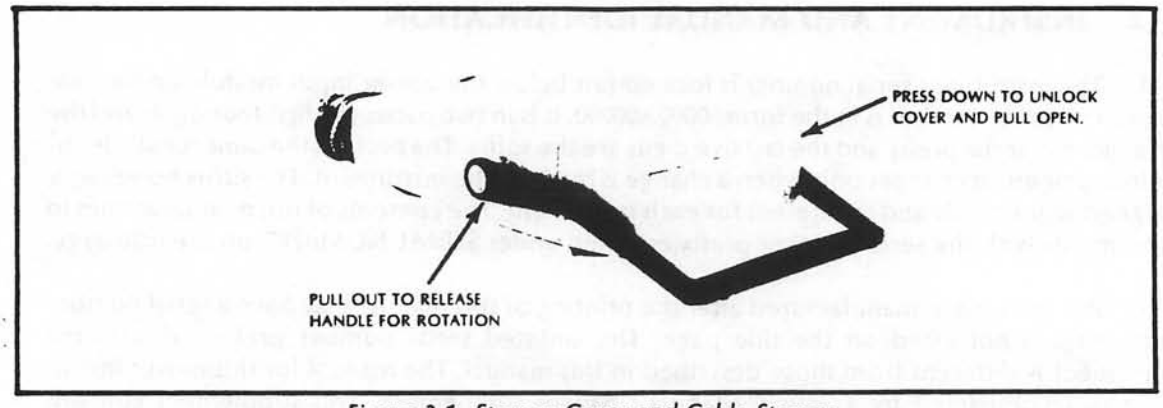


Figure 3-1. Storage Cover and Cable Storage

3-6. FRONT PANEL STORAGE COVER OPENING PROCEDURE

3-7. To open the front panel storage cover, perform the following procedures.

1. Pull gently at both side handle pivot points simultaneously, to unlock and rotate it.
2. Press down to open the front panel storage cover, exposing the 5005A front panel and Data Probe and Pod storage area.

3-8. DATA PROBE AND POD STORAGE

3-9. *Figure 3-2* shows the removable front panel storage cover open with the Data Probe and Pod in the recommended storage positions. The front panel storage cover should be used to store these components when the 5005A is not in use or is being transported.

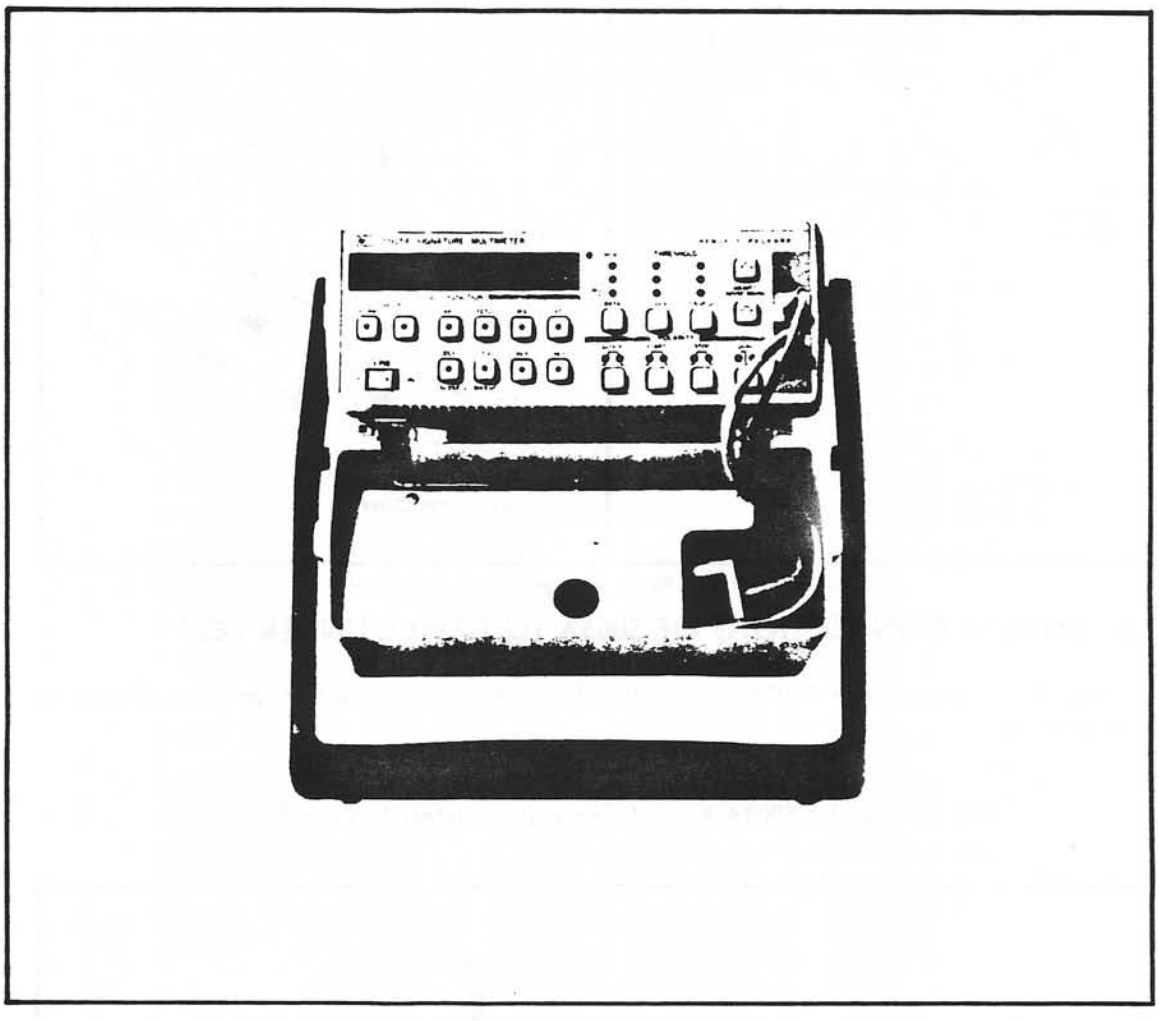


Figure 3-2. Data Probe and Pod Storage

3-10. FRONT PANEL STORAGE COVER REMOVAL PROCEDURE

3-11. To remove the front panel storage cover, perform the following procedures. Refer to *Figure 3-3*.

1. Unhook inside partition from front panel cover and raise the partition up.
2. Press in at one of the sides of the wire hinge-pin and remove inside partition.
3. Remove front panel storage cover.
4. To replace the cover and partition, perform the reverse of the removal procedure.

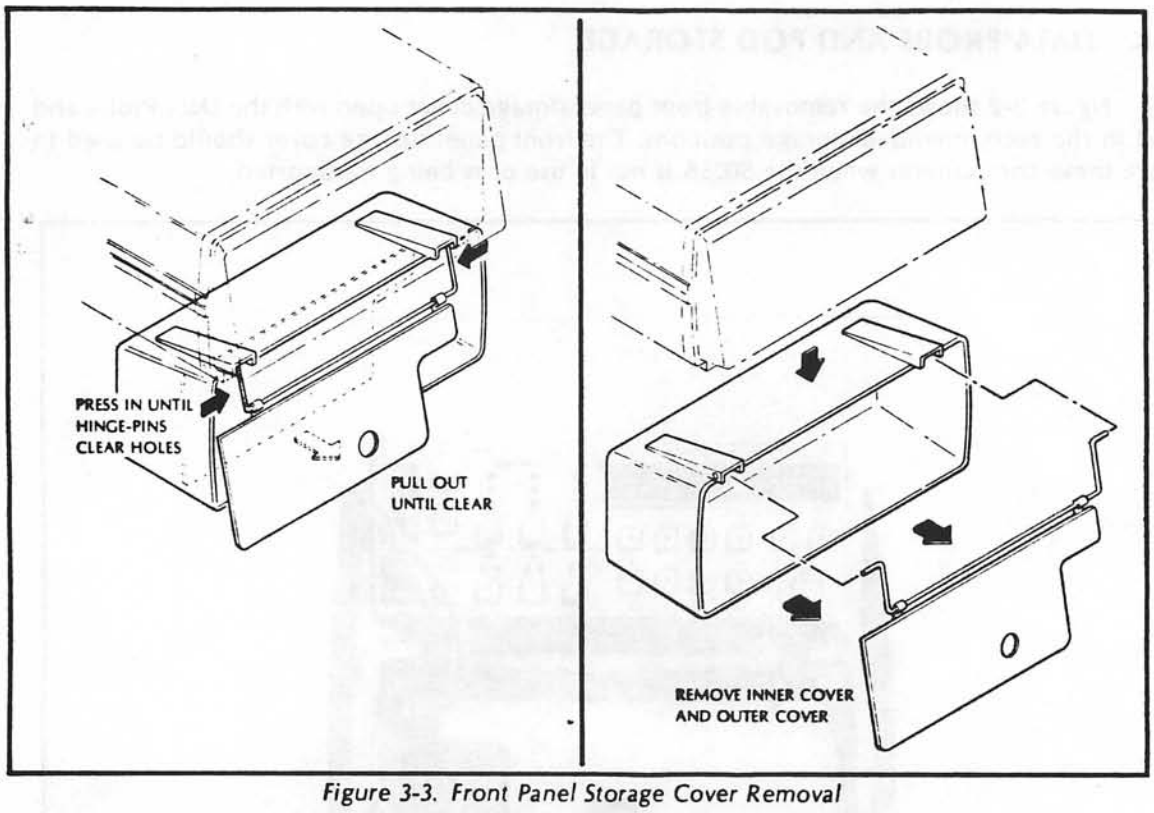


Figure 3-3. Front Panel Storage Cover Removal

3-12. TYPICAL CONNECTIONS OF 5005A TO DEVICE UNDER TEST

3-13. *Figure 3-4* shows the 5005A Signature Multimeter connected to another device to take "signatures."

NOTE

The case of the 5005A is insulating plastic material so it will not cause electrical short circuits.

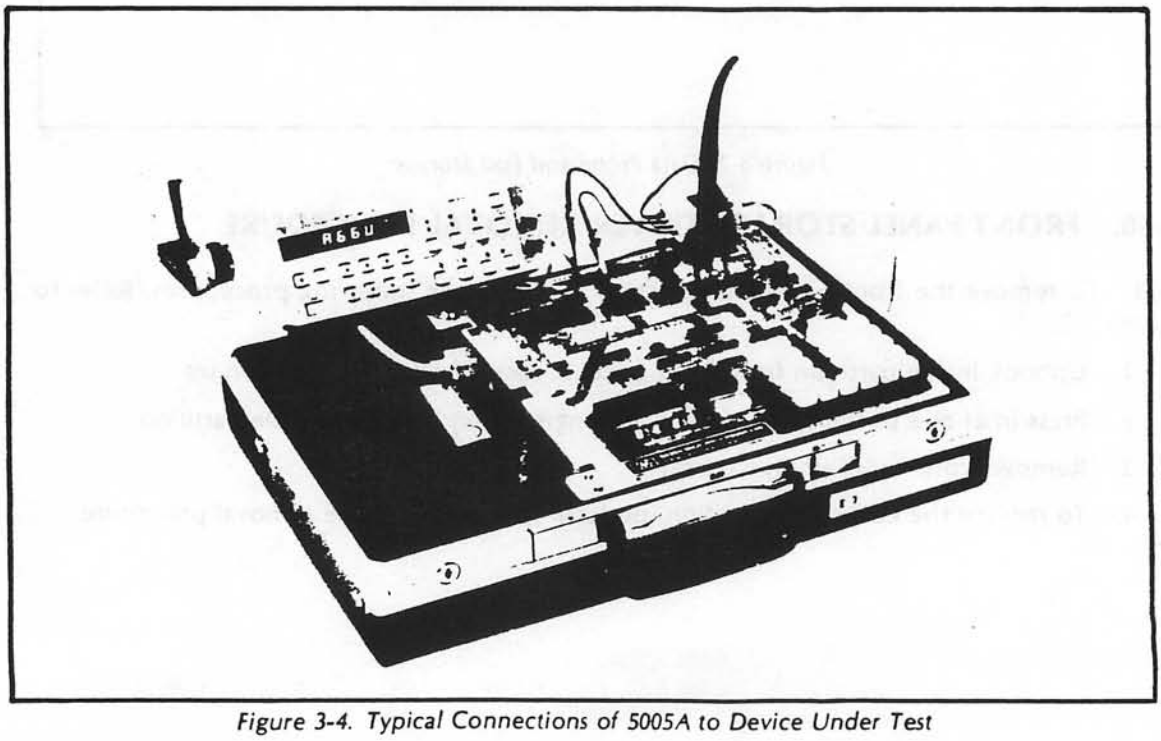


Figure 3-4. Typical Connections of 5005A to Device Under Test

3-14. TEST TERMINAL GRABBER CONNECTIONS

3-15. Five test-terminal grabber connectors are supplied with the 5005A. A grabber can be used on the end of the Timing Pod test leads to make reliable electrical connections from the 5005A to the instrument being tested. To connect a grabber to a test lead of the Pod, simply press the grabber on to the lead as shown in *Figure 3-5*. To place a grabber on the IC pin, grasp the grabber and compress the thumbhold. This allows the metal hook to open and be placed on the desired IC pin. To remove the grabber, compress the thumbhold and remove the grabber from the IC pin. The removable ground (⊥) test lead for the Data Probe also has a grabber.

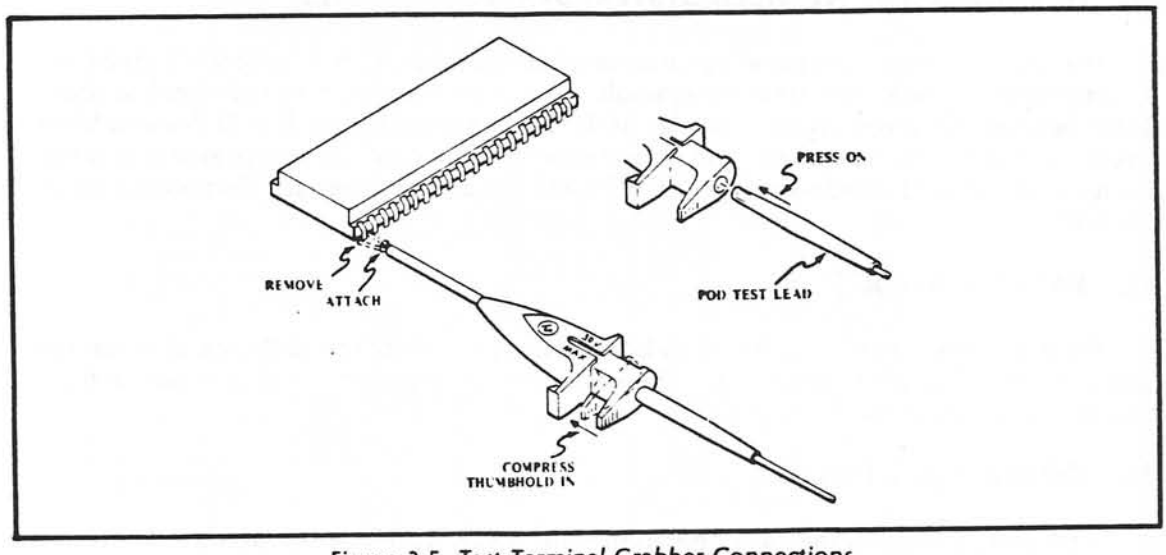


Figure 3-5. Test Terminal Grabber Connections

3-16. SIGNATURE ANALYSIS

3-17. The 5005A Signature Multimeter presents digital signatures with a four-character (symbol) display on its front panel. Each character, which can be any one of 16 symbols, is shown on a 7-segment light-emitting diode (LED) display. The 16 possible characters are:

3-18. The characters presented on the display are special hexadecimal numbers which represent the residue in a CRC (Cyclical Redundancy Code) shift register in the 5005A after START and STOP signals have been received. The number of data bits between the START and STOP signals can be 1 to ∞ (infinity).

NOTE

No signature appearing on the 5005A display has any particular significance beyond being a correct (expected) signature or an incorrect signature. The number is, however, a residue in the 5005A converted to and displayed in special hexadecimal.

3-19. SIGNATURE ANALYSIS LITERATURE

3-20. Further Signature Analysis information literature is listed in *Application Note 222-0, An Index to Signature Analysis Publications.* This maintained document lists the description and part number of the available literature concerning digital Signature Analysis, which can be ordered through the nearest Hewlett-Packard Sales and Service Office.

3-21. HEXADECIMAL NUMBER SYSTEM SYMBOLS (DIGITS)

3-22. The four-character front panel Signature Analysis display presents numbers in a special set of hexadecimal symbols. The final six symbols are not the common hexadecimal symbols ABCDEF because the seven segment display of the 5005A cannot show a B or D that would be different from an 8 or 0 respectively (and several other symbols could be interpreted as another character when viewed upside-down e.g. $\mathcal{E}$ - $\mathcal{E}$). The actual characters are illustrated in paragraph 3-17.

3-23. PANEL FEATURES

3-24. Front and rear panel connectors, indicators, and controls of the 5005A are described in *Figures 3-8, 3-9, 3-10* and *3-11* respectively. These figures locate and describe all operator controls, connectors, and indicators.

3-25. OPERATOR'S CHECKS

3-26. A procedure to verify the basic operation of the 5005A is provided in *Table 3-6*. The check utilizes the instruments self-check cycle and verification of front panel indications. No additional equipment is required.

3-27. POWER-UP SELF CHECK

3-28. When the 5005A is turned-on, a power-up self-check cycle is automatically started. With no inputs applied, the sequence is as follows:

1. Initially, all segments, indicators, and pushbutton LEDs on the front panel and display are lighted except the GATE and UNSTABLE LED's which flash momentarily.
2. Then, after powering-up, the rising edge (CLOCK, START, STOP), the THRESHOLD TTL LED's, and the (NORM) pushbutton LED will light. The display will contain - - - -.

3-29. During this cycle, the microprocessor performs a check sum of the internal program in ROM and a bit pattern is written into and read from RAM. Additionally, a timer test, DVM test, internal count test, LED test, and a partial check of the D/A converter circuits are performed. A failure during the cycle will display a numbered error message, or will result in a visibly improper state of the front panel display and indicators. Refer to Error Messages, paragraph 3-34.

3-30. QUICK OPERATION TEST

3-31. The Quick Operation Test verifies other circuits not checked in the Power-Up Self-Check. The procedure is as follows:

1. Press the (kΩ) pushbutton on the front panel. Verify that the display reads O P E N.

2. Connect Data Probe tip to the Timing Pod START/ST-SP (green), STOP/QUAL (red), and CLOCK (yellow) leads sequentially. Verify that the display reads approximately 100K ohms for each reading.
3. Connect Data Probe tip to the Timing Pod ground (black) lead. Verify that the display reads zero ohms.

3-32. CONDITIONAL DISPLAYS

3-33. Under certain circumstances the HP5005A will respond with a unique display, representative of a special condition. The possible conditional displays and the indicated meaning are listed in *Table 3-1* below.

Table 3-1. Conditional Displays

Function Mode	Display	Meaning
Signature Analysis NORM QUAL	- - - -	No measurement taken.
kHz	O F L O	Measurement overflow, input frequency ≥ 100 MHz.
TOTLZ	O F L O	Measurement overflow, events totalized > 99,999 counts.
ms	O F L O	Measurement overflow, time interval > 99,999 ms.
Vp+, Vp–	O L	Voltage peak ≥ 12.5 volts.
Vp+, Vp–	–O L	Voltage peak ≤ –12.5 volts.
⚠ DCV	O L –O L	Voltage ≥ 260 volts. Voltage ≤ –260 volts.
⚠ ΔV	O L –O L	Voltage of one reference point ≥ 260 volts. Voltage of one reference point ≤ –260 volts.
kΩ	O L –O L O L –O L O P E N	Drastic overload: ≈ 20 volts or greater. Positive source 2 volts connected. Negative source 2 volts connected. Open circuit.
All	ERRXX	Internal error with identifying number.

3-34. ERROR MESSAGES

3-35. Failures during the Power-Up Self-Test will result in a display of a numbered error message. There are 16 numbered Error Messages, as listed below. Refer to Section VIII in the Service Manual for additional information.

ERROR	MESSAGES
ERR00	ROM checksum error
ERR04	RAM read/write error
ERR06	Timer error
ERR07	DVM Zero offset measurement exceeds ±00200
ERR08	DVM data exceeds 32000
ERR09	DVM 10V calibration measurement exceeds 10.3V on 25V range
ERR10	DVM 10V calibration measurement is less than 9.3V on 25V range
ERR11	DVM 10V calibration measurement exceeds 10.3V on 250V range
ERR12	DVM 10V calibration measurement is less than 9.3V on 250V range

ERR13	Ohms 2V calibration exceeds 2.1V
ERR14	Ohms 2V calibration less than 1.9V
ERR15	Internal count test or keyboard error (illegal keycode)
ERR16	D/A converter Zero Offset exceeds 200 mV
ERR18	DVM measurement timeout — M/Z status incorrect
ERR19	DVM data transfer error-digit strobe status incorrect
ERR20	Keyboard encoder DATA VALID signal error

3-36. INSTRUMENTS COMPATIBLE WITH 5005A.

3-37. The 5005A is used to test the operation of electronic digital logic products with the signature analysis method.

3-38. OPERATING INSTRUCTIONS

WARNING

BEFORE THE INSTRUMENT IS SWITCHED ON, ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, AUTO TRANSFORMERS, AND DEVICES CONNECTED TO IT SHOULD BE CONNECTED TO A GROUNDED SOCKET. ANY INTERRUPTION OF THE PROTECTIVE EARTH GROUNDING WILL CAUSE A POTENTIAL SHOCK HAZARD THAT COULD RESULT IN PERSONAL INJURY.

WARNING

THE GROUND TEST LEADS ON THE POD AND DATA PROBE ARE TIED TO THE CHASSIS GROUND OF THE INSTRUMENT AND SHOULD NOT BE CONNECTED TO A VOLTAGE OTHER THAN GROUND FOR MEASUREMENTS.

WARNING

ONLY FUSES WITH THE REQUIRED RATED CURRENT AND SPECIFIED TYPE SHOULD BE USED. DO NOT USE REPAIRED FUSES OR CIRCUITED FUSE-HOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.

CAUTION

Before the instrument is turned on, the Line Module must be set to match the voltage of the power line, or damage to the instrument could result.

3-39. The 5005A makes analog measurements; DCV, ΔV, Vp+, Vp–, kΩ, and digital measurements; NORM, QUAL kHz, TOTLZ, ms. In all digital modes, the 5005A interprets input signal levels according to the thresholds set. That is, the thresholds define the logic levels for the incoming signals.

3-40. General Set-Up Procedures

3-41. The general set-up procedures described below are to be used prior to performing the measurement set-ups in *Tables 3-7* through *3-15*.

1. Set the 5005A LINE switch to ON. The 5005A performs a power-up self-check and goes into NORM mode. (See paragraph 3-27.)
2. Select the desired FUNCTION pushbutton.
3. Select and set the THRESHOLD, if required.
4. Select and set the POLARITY edges or QUAL level, if required.
5. Connect the Timing Pod leads to the signals to be measured, if required.

3-42. Programming the Input Logic Levels

3-43. The 5005A is pre-programmed to trigger on standard logic thresholds. The 5005A automatically powers-up in the TTL logic family mode and triggers at the voltage values listed in *Table 3-2*. The logic family mode for DATA (Probe), CLOCK (Pod), and ST-SP-QL (Pod) can be changed by pressing the pushbutton corresponding to that input. To change from one logic family to another, press the appropriate threshold pushbutton (DATA, CLOCK, or ST-SP-QL) in rapid succession until the logic family (TTL, ECL, CMOS 5V) LED lights. The following examples describe this procedure.

1. Press the DATA pushbutton three times in succession. The first press displays the TTL High DATA THRESHOLD level (2.00H). The second press displays the TTL Low DATA THRESHOLD level (0.80L). The third press changes the DATA logic threshold levels to the next logic family (ECL) and displays the High DATA THRESHOLD level for that logic family (-1.10H). The programmed logic levels for the selected input (DATA, CLOCK, or ST-SP-QL) can be reviewed at any time by pressing the respective pushbutton once for the High level, and once more for the Low level. If no pushbuttons are pressed for approximately 2 seconds, the display will return to the previously set operating mode.
2. Press the CLOCK pushbutton two times in quick succession. The first press displays the CLOCK THRESHOLD TTL trigger level. The second press changes the CLOCK logic threshold level to the next logic family (ECL), and displays the new CLOCK THRESHOLD trigger level (-1.30).
3. Press the ST SP-QL pushbutton two times in quick succession. The first press displays the ST-SP-QL THRESHOLD TTL trigger level. The second press changes the ST-SP-QL logic threshold level to the next logic family (ECL) and displays the new ST-SP-QL THRESHOLD trigger level (-1.30).

Table 3-2. Logic Family Voltage Levels

FUNCTION	THRESHOLDS		
	TTL	ECL	5V CMOS
DATA	H 2.00V	-1.10V	3.50V
	L 0.80V	-1.50V	1.50V
CLOCK	1.40V	-1.30V	2.50V
ST-SP-QL	1.40V	-1.30V	2.50V

3-44. Threshold Level Setting and Adjustment

3-45. To change the value of a programmed threshold, within any logic family, the appropriate input threshold pushbutton (DATA, CLOCK, or ST-SP-QL) should be pressed until the level to be changed is displayed. An H or L will follow the displayed DATA THRESHOLD setting indicating the High or Low logic level currently set. To change the levels once the family (an H or L level for DATA) is selected, the ⇧ or ⇩ ADJUST/NOISE MARG pushbuttons are pressed, slewing the levels up or down respectively. The display will contain the current setting of the selected level. Setting and adjusting the input THRESHOLD levels is the same procedure for all measurement modes of the 5005A. For this reason, the following examples are given only for the NORM Signature Analysis mode. Refer to *Table 3-3* to indicate what THRESHOLD pushbuttons are active in each measurement mode.

1. To modify any of the input THRESHOLDs (High or Low DATA, CLOCK or ST-SP-QL) in any of the three logic families (TTL, ECL CMOS 5V, that THRESHOLD has to be displayed. This is done by pressing the corresponding THRESHOLD pushbutton, DATA, CLOCK, or ST-SP-QL until the required family LED is lighted and the threshold voltage is displayed; High or Low in case of DATA THRESHOLDS.
2. While the threshold voltage is displayed, it can be changed by pressing ⇧ or ⇩ ADJUST/NOISE MARG pushbuttons. A single depression will cause a 50mV step change, while holding the pushbutton down will cause a repeated stepping up or down with increasing speed. The maximum threshold voltage that can be set is ±12.5V. If no pushbuttons are pressed for approximately 2 seconds, the display will return to the previously set operating mode.
3. Whenever a threshold value, different from the preset (standard) value is displayed, the UNCAL (uncalibrated) LED will be lighted. The UNCAL LED will also be lighted in any measurement mode using one or more non-standard thresholds.

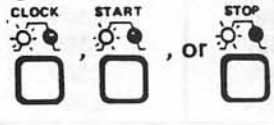
Table 3-3. Thresholds Used in Each Function

FUNCTION	THRESHOLDS		
	DATA	CLOCK	ST-SP-QL
NORM	*	*	*
QUAL	*	*	*
kHz	*		
TOTLZ	*		*
ms			*

*Indicates that particular THRESHOLD pushbutton is active.

3-46. Polarity Setting and Change

3-47. The procedure for setting and changing the POLARITY edges or level is contained in the following instructions. Refer to *Table 3-4* to indicate what POLARITY pushbuttons are active in each measurement mode.

1. To change the POLARITY edges (CLOCK, START, or STOP), the corresponding push-button 

is pressed and the desired edge-select LED is lighted.

2. To change the POLARITY level (QUAL), the corresponding pushbutton 

is pressed and the desired level LED is lighted. The left LED indicates High level active, and the right LED indicates Low level active.

Table 3-4. Polarities Used in Each Function

FUNCTION	POLARITY			
	CLOCK	START	STOP	QUAL
NORM	*	*	*	
QUAL	*	*	*	*
TOTLZ		*	*	
ms		*	*	

*Indicates that particular POLARITY pushbutton is active. POLARITY pushbuttons are active only in the four listed functions.

3-48. MEASUREMENT PROCEDURES

3-49. The following paragraphs describe the general measurement functions of the 5005A Signature Multimeter. *Tables 3-7* through *3-15* show general operating procedures with the 5005A in typical measurement setups.

3-50. Signature Analysis Measurements (NORM)

3-51. The 5005A can make Signature Analysis measurements on TTL, ECL, and 5V CMOS logic families. In addition, the threshold can be set to any level between –12.5V to +12.5V to make measurements on other logic families. The maximum input data rate is 20 MHz.

NOTE

Each measurement function of the 5005A is selected by pressing its function pushbutton. If any threshold or polarity settings are relevant to this measurement, the corresponding LEDs will be lighted.

3-52. Signature Analysis Measurements (QUAL)

3-53. The 5005A Signature Analysis measurements can be enhanced with the Signature QUAL mode. The QUAL input, on the Timing Pod, is sensed by the 5005A as a Data Qualifier. Conceptually, the qualifier can be thought of as an "enable" signal. See *Figure 3-6* The active qualified level (logic low or high) can be selected by the QUAL pushbutton. The START and STOP polarities can still be individually selected with the POLARITY pushbuttons. When in the QUAL Signature mode, the red Timing Pod lead becomes the QUAL (qualifier) input and the green timing Pod lead becomes the START **and** STOP input.

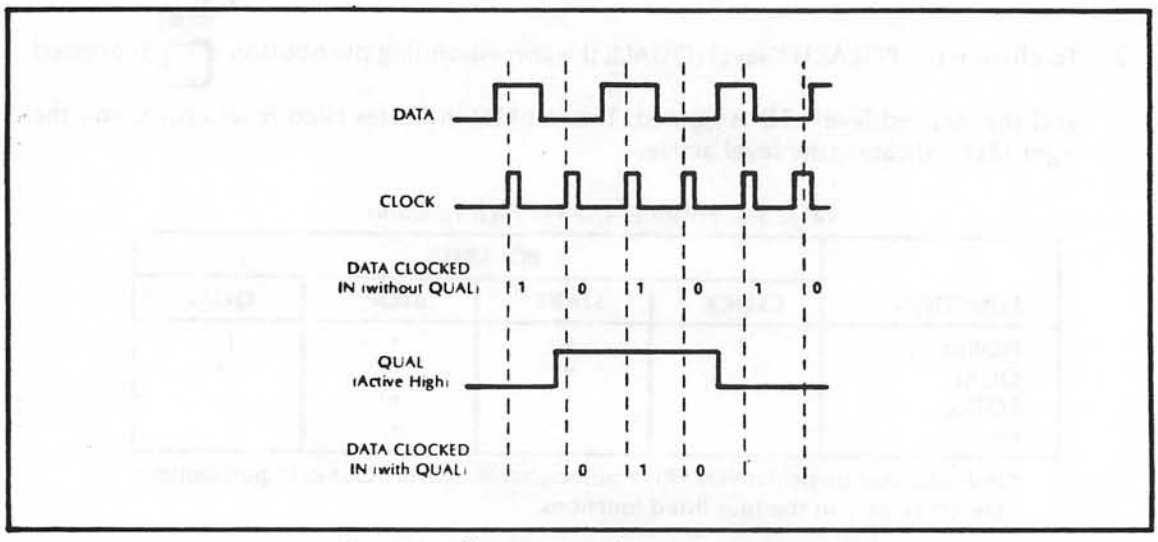


Figure 3-6. Signature Analysis Measurements

3-54. Frequency Measurements

3-55. The 5005A makes frequency measurements, using TTL, ECL, and CMOS logic family thresholds, on input signals within the range of 0 to 50 MHz. These frequencies are counted directly with no prescaling techniques applied. The measurement gate time is fixed at one second. This gives a resolution of 1Hz up to 100kHz where the resolution becomes 1 LSD at a 5 digit display. The accuracy is ±0.01% of reading ±1 count.

3-56. Totalize Measurements

3-57. The 5005A can count the number of pulses occuring at the Data Probe between the START and STOP timing signals. In this mode, all the inputs (Start, Stop, and Data) are used asynchronously. The Clock input is not used. In the totalize mode, the 5005A can accumulate from 0 to 99,999 counts at a maximum rate of 50 MHz. *Figure 3-7* illustrates the timing relationship in the totalize measurement mode of operation.

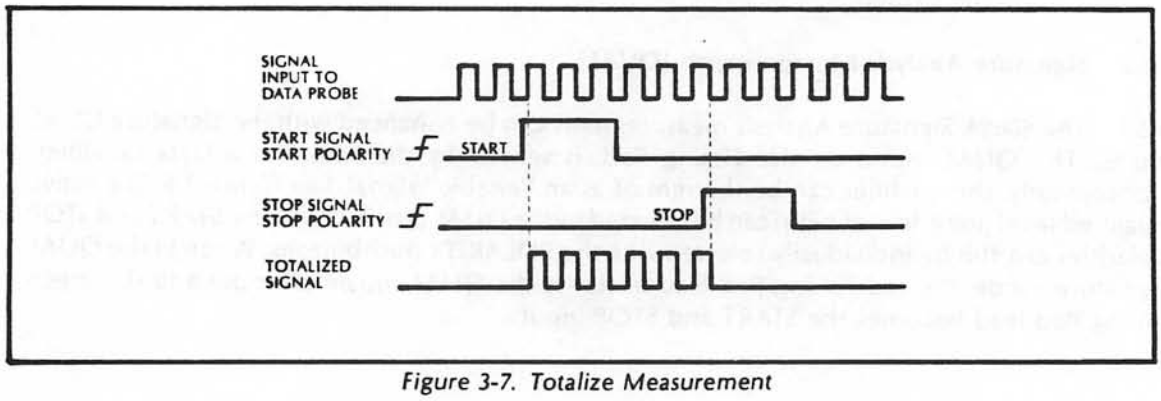


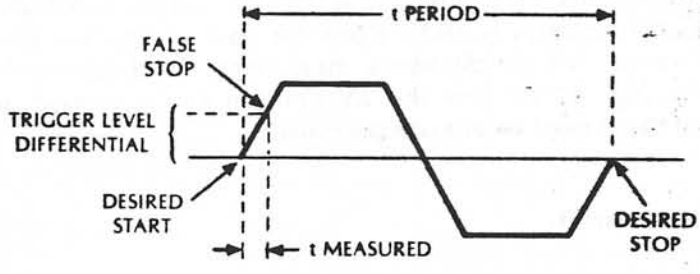
Figure 3-7. Totalize Measurement

3-58. Time Interval Measurements

3-59. Time interval measurements are made between a selected transition at the START lead and a consecutive transition on the STOP lead. The range is from 0 to 99,999 milliseconds with an accuracy of ±0.01% of reading ±1 count. Two source time interval measurements are displayed on a 5-digit display with a resolution of 100 ns.

NOTE

The Start and Stop trigger thresholds are connected together internally, but differences do exist in the trigger circuitry. This results in a small differential between the Start and Stop trigger levels. This condition allows the possibility of unexpected measurements during the Time Interval mode. For example:



For Time Interval measurements, the expected result would be the period (t period) of the input sinewave. However, depending on the trigger level differential, an unexpected measurement (t measured) may result.

3-60. Volts Peak, Plus or Minus Measurements

3-61. Peak voltages can be measured between ±12.0V provided the peak duration is ≥10ns and the rate is ≥20 Hz. The 3 1/2-digit display provides a resolution of 50mV with an accuracy of ±2% of reading ±5% of p-p signal ±100 mV.

⚠ 3-62. DC Volt Measurements

3-63. The 5005A can measure a maximum of ±250 VDC with a 10M input impedance and features auto ranging and auto polarity circuits. The 4 1/2-digit display gives a resolution of 1mV up to 25V, 10mV from 25V to 100V and 100mV from 100V to 250V. The accuracy is ±0.1% ±2mV up to 25V and ±0.25% ±20mV from 25V to 250V.

⚠ 3-64. Delta Volt Measurements

3-65. The 5005A can measure a difference in voltage levels up to ±250V (maximum differential 500V) with an input impedance of 10M. The 4 1/2-digit display gives a resolution of 1mV if both voltages are less than 25V, 10mV if the difference is from 25V to 100V, and 100mV if the difference is from 100V to 250V. The accuracy is ±0.1% ±2mV for both voltages less than 25V and ±0.25% otherwise. The "reference" for the difference measurement is determined from the voltage present at the probe (tip) at the time the ΔV function key is pressed. **In this mode, the Data Probe ground (if used) must be at earth potential.**

3-66. Resistance Measurements

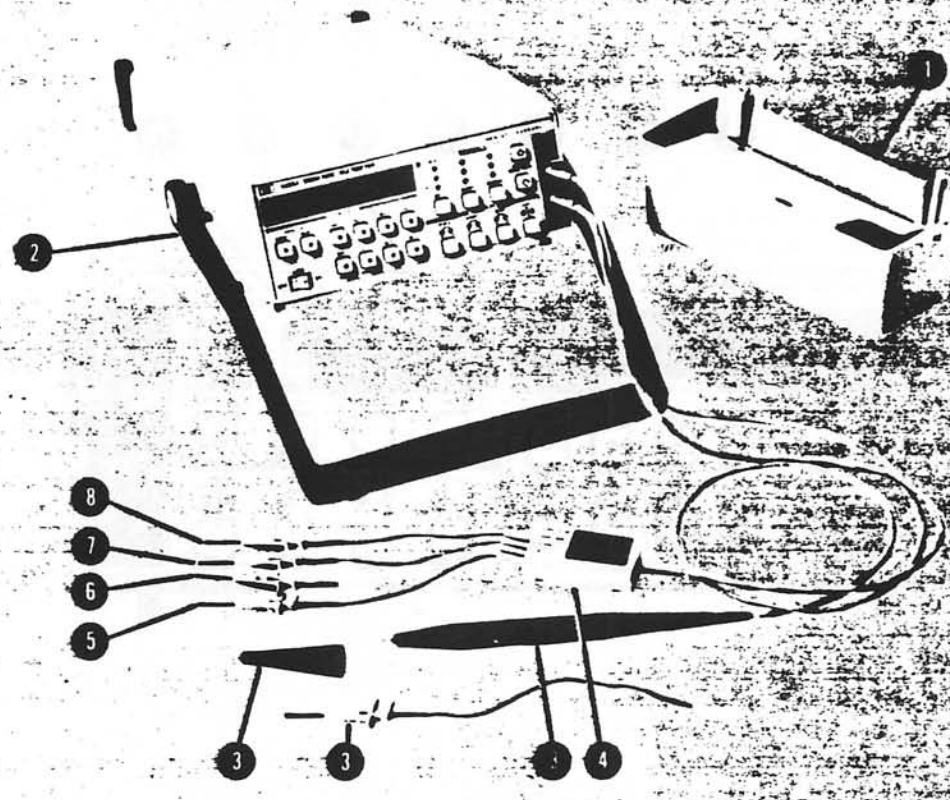
3-67. Resistance measurements can be made from 0 to 10MΩ. The resolution and accuracy are given in *Table 1-1*.

3-68. OPERATOR'S MAINTENANCE

3-69. The only maintenance the operator should normally perform is the replacement of the primary fuse on the 5005A. This fuse is located within the A7 Line Module Assembly. For instructions on how to change the fuse, refer to Section II, Line Voltage Selection.

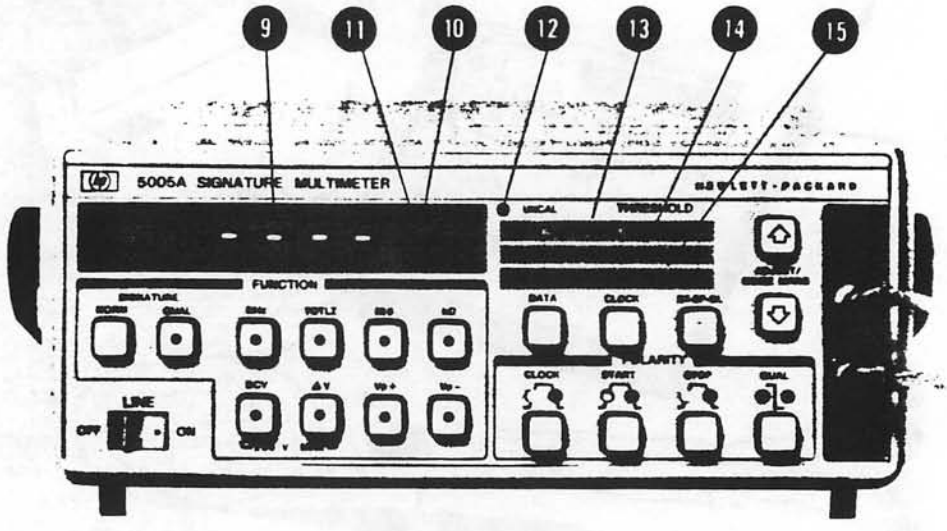
CAUTION

Make sure that only fuses with the required rated current and of the slow-blow type are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.



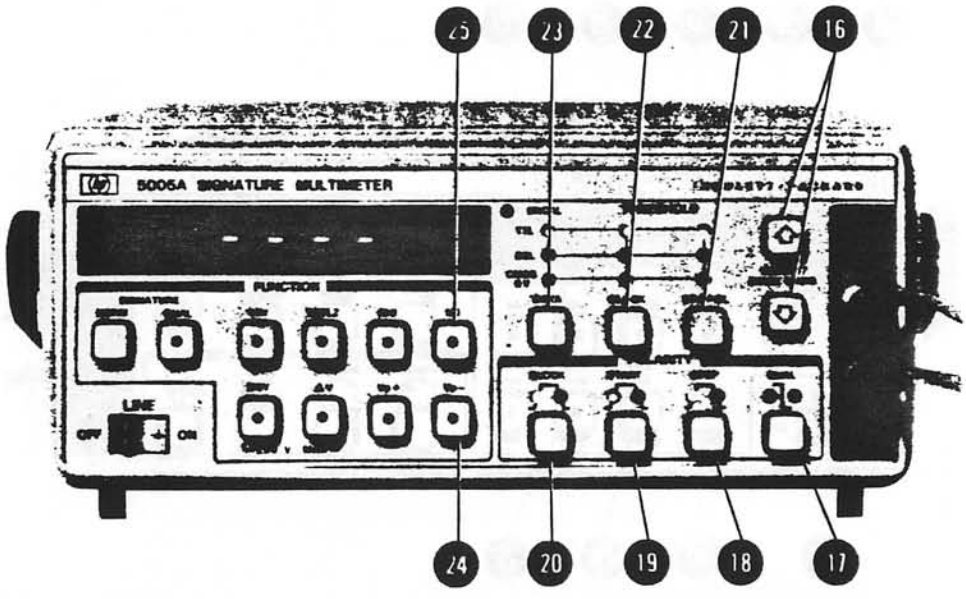
1	**STORAGE COVER**	Storage for the Data Probe, Timing Pod, and grabbers.
2	**HANDLE STAND**	The combination handle and stand can be rotated by gently pulling at both handle pivot points simultaneously and turning the handle to the desired position.
3	**DATA PROBE, PROTECTIVE COVER, and GND LEAD**	Point of entry for data from the unit being tested by the 5005A. The lamp above the probe tip indicates logic state of the data: On Bright=High, On Dim=Three-state, Off=Low. 10ns or greater pulses are stretched to 100ms. Note Probe ground connector (measuring earth terminal) and protective cap cover for Probe. Note that the probe acts as a logic probe in the SA, QUAL, kHz, and TOTLZ modes. The lamp has an undefined meaning in the DCV, VP+, VP-, ms, and ΔV modes.
4	**TIMING POD**	Four timing inputs, START/ST-SP, STOP/QUAL, CLOCK, and a common ground (⊥) are for connection to a Unit Under Test.
5	**GND POD LEAD**	Common (ground) lead (measuring earth terminal) for connection to Unit Under Test.
6	**CLOCK POD LEAD**	Point of entry for CLOCK signal from the Unit Under Test.
7	**STOP/QUAL POD LEAD**	Point of entry for STOP signal in NORM mode and QUAL signal in QUAL mode from the Unit Under Test.
8	**START/ST-SP POD LEAD**	Point of entry for START signal in NORM or QUAL mode and STOP and START signals in QUAL mode from the Unit Under Test.

Figure 3-8. Signature Multimeter, Probe and Pod Features



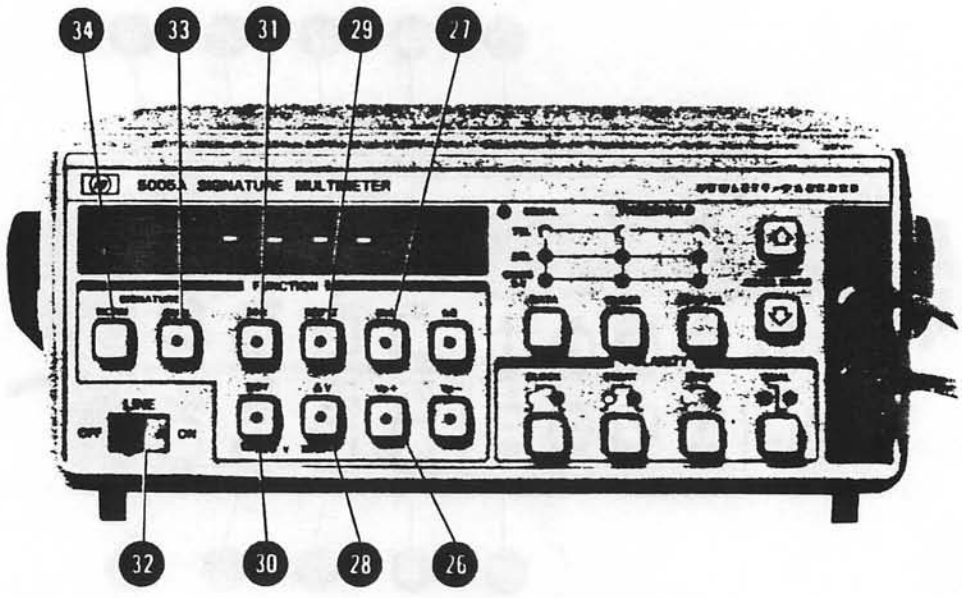
9	**DISPLAY**	Contains the five seven-segment LED displays, and the preceding minus sign.
10	**GATE LED**	Flashing of GATE LED indicates 5005A is being gated.
11	**UNSTABLE LED**	Indicates an unstable signature reading.
12	**UNCAL LED**	Indicates that one or more of currently used input threshold levels is adjusted to a non-standard value.
13	**TTL LEDs**	Indicates the respective thresholds are set to test TTL logic. The TTL LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.
14	**ECL LEDs**	Indicates the respective thresholds are set to test ECL logic. The ECL LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.
15	**CMOS LEDs 5V**	Indicates the respective thresholds are set to test 5V CMOS logic. The 5V CMOS LED will be lighted even if the thresholds have been modified by the user. The UNCAL LED will light to indicate this condition.

Figure 3-9. Front Panel Indicators



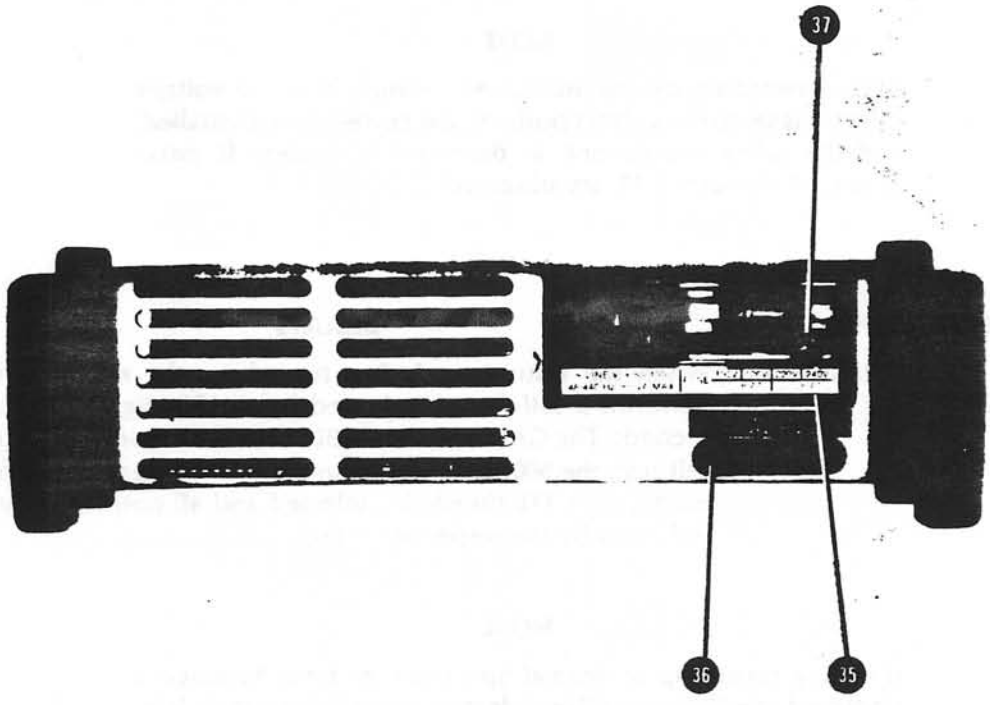
16	ADJUST NOISE MARG	Voltage threshold adjustment by single steps (or continuously if pressed-in and held) up or down in increments of 50 mV. Threshold adjustment pushbuttons can be used to check noise margins in the tested logic circuit.
17	**QUAL**	Selects whether the signature analysis is enabled by high or low level of the qualifying signal.
18	**STOP**	These three pushbuttons select either the positive-going or negative-going transition of the input signals to be used for timing of the measurements.
19	**START**	
20	**CLOCK**	
21	**ST-SP-QL (Start-Stop-Qual)**	This switch programs the ST-SP-QL inputs to operate with TTL, ECL, or 5V CMOS logic families.
22	**CLOCK**	This pushbutton programs the CLOCK input to operate with TTL, ECL, or 5V CMOS logic families.
23	**DATA**	This pushbutton programs the DATA input to operate with TTL, ECL, or 5V CMOS logic families.
24	**Vp–**	This pushbutton activates the negative peak voltage measurement.
25	**kΩ**	This pushbutton activates the resistance measurement. The measured resistance must be placed between the Data Probe tip and the Pod or Data Probe ground.

Figure 3-10. Front Panel Controls



26	**Vp+**	This pushbutton activates the positive peak voltage measurement.
27	**ms**	The ms pushbutton activates the time interval measurements between the START and STOP signals at the Timing Pod leads.
28	**ΔV**	The delta volt pushbutton activates the 5005A to measure voltage levels at the Data Probe referenced to the voltage at the Data Probe at the time the ΔV pushbutton was pressed.
29	**TOTLZ**	This pushbutton activates the 5005A for counting the number of pulses at the input to the Data Probe occurring between the START and STOP pulses at the input to the Timing Pod.
30	**DCV**	The DCV pushbutton activates the 5005A to measure the voltage at the Data Probe tip referenced to ground.
31	**kHz**	The kHz pushbutton activates the 5005A for frequency measurements.
32	**LINE ON-OFF**	This is the main line switch for power to the 5005A.
33	**QUAL**	The QUAL pushbutton activates the 5005A for signature analysis in the qualified mode. The CLOCK, START, STOP edges, and QUAL level as well as the logic thresholds are programmable in this mode.
34	**NORM**	The NORM pushbutton activates the 5005A for signature analysis in the normal mode. The CLOCK, START, and STOP trigger edges as well as the logic thresholds are programmable in this mode.

Figure 3-10. Front Panel Controls (Continued)



35 The ac power input module permits operation with 100, 120, 220, or 240 volts ac. The number visible in the window indicates nominal line voltage to which instrument must be connected (see *Figure 2-1*). Protective grounding conductor connects to the instrument through this module.

36 This external connector provides three +5V sources to power the HP545A Logic Probe, the HP546A Logic Pulser, the HP547A Current Tracer, or the HP5001A Microprocessor Exerciser.

37 Fuse-Pull.

Figure 3-11. Rear Panel Features

Table 3-5. Operator Checks

OPERATOR CHECKS PROCEDURE

NOTE

Before switching on the instrument, ensure that the voltage selector is set to the correct position, the correct fuse is installed, and the safety precautions, as described in Section II, paragraph 2-5 through 2-11, are observed.

STEP	PROCEDURE	RESULTS
1.	Set 5005A LINE switch to ON.	When the instrument is first turned-on, the microprocessor performs a self-test as indicated by all LEDs lighted for a few seconds. The GATE and UNSTABLE LEDs flash momentarily. After self-test, the 5005A should be in the NORM Signature Analysis mode, with TTL thresholds selected and all positive polarities indicated by the respective LEDs.
	NOTE	
	If during power-up or normal operation, an Error Message is displayed, the 5005A could be defective. Refer to Paragraph 3-34, ERROR MESSAGES, in this section.	
2.	Press Ω •	Ω ☼ pushbutton LED lights. 5005A displays O P E N.
3.	Connect Data Probe tip to the Pod START/ ST-SP (green), STOP/ QUAL (red) and CLOCK (yellow) leads sequentially.	5005A measures approximately 100kΩ for each lead.
4.	Connect Data Probe tip to the Pod ground (black) lead.	5005A measures 0± .002.

Table 3-6. NORM Signature Analysis Measurement

NORM SIGNATURE ANALYSIS MEASUREMENT PROCEDURE

NOTE

Correct (expected) signatures for the Device Under Test (DUT) must be known for proper use of the 5005A. Signatures will usually be listed in the troubleshooting section of the DUT manual.

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press NORM.	NORM pushbutton lights.
2.	Connect START/ST-SP, STOP/QUAL, CLOCK, and Pod ground (⊥) leads to specified test points of the DUT. (Refer to DUT manual.)	
3.	Set DATA, CLOCK, and ST SP-QL to the Logic family indicated in DUT manual.	Corresponding LEDs light.

NOTE

If the DUT manual specifies a 5004A Signature Analyzer, select only the preset TTL THRESHOLD levels.

4.	Set CLOCK, START, and STOP edges as stated in DUT manual.	Specified edges toggle and LEDs light. GATE light indicates gating.

Table 3-6. NORM Signature Analysis Measurement (Continued)

NORM SIGNATURE ANALYSIS MEASUREMENT PROCEDURE (Continued)

5.	The set-up can be checked by probing Vcc for an expected signature.	5005A displays Vcc signature.
6.	Connect Data Probe to the tested node of DUT.	5005A displays test signatures to be compared with those in DUT manual.

NOTE

The first two signatures displayed may be wrong, which is noticable when slow gating is used. In this condition the UNSTABLE LED will light and the signatures should be ignored. When a signature, which is different from the preceeding signature is displayed, the UNSTABLE LED lights. The first correct signature (following an incorrect signature) will have the UNSTABLE LED lighted. Only at the second correct signature will the UNSTABLE LED turn-off. The 5005A has to read at least two identical stable signatures before the UNSTABLE LED will turn-off as indicated below.

DISPLAYED SIGNATURE	INCORRECT	INCORRECT	CORRECT	CORRECT	CORRECT
UNSTABLE LED	ON	ON	ON	OFF	OFF

Table 3-7. QUAL Signature Analysis Measurement

QUAL SIGNATURE ANALYSIS MEASUREMENT PROCEDURE

NOTE

Correct (expected) signatures for the Device Under Test (DUT) must be known for proper use of the 5005A. Signatures will usually be listed in the troubleshooting section of the DUT manual.

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press QUAL .	QUAL pushbutton lights.
2.	Connect START/ST-SP STOP/QUAL, CLOCK, and Pod ground (⊥) leads to specified test points of the DUT. (Refer to DUT manual.)	
3.	Set DATA , CLOCK , and ST-SP-QL to the Logic family indicated in DUT manual.	Corresponding LEDs light.
4.	Set CLOCK , START , STOP edges and QUAL level as in DUT manual.	Specified edges toggle and LEDs light. GATE light indicates gating.
5.	The set-up can be checked by probing Vcc for an expected signature.	5005A displays Vcc signature.

Table 3-7. QUAL Signature Analysis Measurement (Continued)

QUAL SIGNATURE ANALYSIS MEASUREMENT PROCEDURE (Continued)

6.	Connect Data Probe to the tested node of DUT.	5005A displays test signatures to be compared with those in DUT manual.

NOTE

The first two signatures displayed may be wrong, which is noticable when slow gating is used. In this condition, the UNSTABLE LED will light and the signatures should be ignored. When a signature, which is different from the preceeding signature is displayed, the UNSTABLE LED lights. The first correct signature (following an incorrect signature) will have the UNSTABLE LED lighted. Only at the second correct signature will the UNSTABLE LED turn-off. The 5005A has to read at least two identical stable signatures before the UNSTABLE LED will turn-off as indicated below.

DISPLAYED SIGNATURE	INCORRECT	INCORRECT	CORRECT	CORRECT	CORRECT
UNSTABLE LED	ON	ON	ON	OFF	OFF

Table 3-8. Frequency Measurement

FREQUENCY MEASUREMENT PROCEDURE

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press kHz.	kHz pushbutton lights. Gate LED flashes at the fixed 1Hz gating rate.
2.	Set DATA to desired logic family.	Selected logic family LED lights.
3.	Ensure one of the ground (⊥) leads is connected to the DUT ground. For frequencies above 10MHz, the Data Probe ground (⊥) lead should be used.	

NOTE

The frequency measured gate time is fixed at one second as indicated by the flashing GATE LED at the right of the display.

4.	Place the Data Probe tip on the signal to be measured.	Display shows the measured frequency with the GATE LED flashing at the measurement rate.

Table 3-9. Totalize Measurement

TOTALIZE MEASUREMENT PROCEDURE

NOTE

The Logic probe is active in this mode.

STEP	PROCEDURE	RESULTS
1.	Press TOTLZ.	TOTLZ pushbutton lights.
2.	Set DATA and ST-SP-QL to desired logic family.	Selected logic family LEDs light.
3.	Set desired START and STOP edges.	Selected edges toggle and LEDs light.
4.	Connect the Pod START/ST-SP and STOP/QUAL leads to the START and STOP signals.	
5.	Connect the Pod ground (⊥) lead to the ground of the DUT.	GATE light indicates gating.
6.	Place the Data Probe tip on the signal to be totalized.	Display shows the number of pulses occurring during the time between the Start and Stop edges.

Table 3-10. Time Interval Measurement

TIME INTERVAL MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press ms .	ms pushbutton lights.
2.	Set ST-SP-QL to desired logic family.	Selected logic family LED lights.
3.	Set desired START and STOP edges.	Selected edges toggle and LEDs light.
4.	Connect the Pod ground (⊥) lead to the ground of the DUT.	GATE light indicates gating.
5.	Connect the Pod START/ST-SP and STOP/QUAL leads to the START and STOP signals to be measured.	Display shows the time interval between selected transitions of the START and STOP signals.

Table 3-11. Resistance Measurement

RESISTANCE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press Ω [•].	Ω [☼] pushbutton lights. If the Data Probe is not connected, the 5005A displays O P E N.

CAUTION

Before taking resistance measurements ensure the tested circuit is not under power and disconnected from the earth ground. This can normally be done by disconnecting the AC power cord.

2.	Connect Data Probe ground (⊥) lead on one side of resistance to be measured.	
3.	Place Data Probe tip on other side of resistance to be measured.	Display shows the measured resistance between the Data Probe tip and ground.

Table 3-12. Voltage Measurement

VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press DCV [•].	DCV [☼] pushbutton lights.
2.	Connect Data Probe or Pod ground (⊥) lead to the common ground point of source to be measured.	
3.	Place Data Probe tip on voltage point to be measured.	Display shows the measured voltage between the Data Probe and ground.

CAUTION

The Ground input of the DVM is attached to earth ground via the instrument chassis. Do not connect to any voltage other than earth ground.

Table 3-13. Delta Voltage Measurement

DELTA VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Connect Data Probe or Pod ground (⊥) lead to the common ground point of source to be measured.	
2.	Place Data Probe tip on circuit point to be used as a voltage reference point. Press Δv [•]. Hold Data Probe on voltage reference until a numeric display (≈ 0.000) appears.	Δv [-0-] pushbutton lights. 5005A displays zero voltage difference. This is the reference voltage for the following difference measurements.
3.	Place Data Probe tip on the circuit point whose voltage is to be measured.	Display shows the voltage difference between the currently probed circuit point and the previously defined reference (step 2) point.

Table 3-14. Peak Voltage Measurement

PEAK VOLTAGE MEASUREMENT PROCEDURE

NOTE

The Logic probe is not active in this mode and any activity by the lamp should be ignored.

STEP	PROCEDURE	RESULTS
1.	Press V_{P+} or V_{P-}.	Selected pushbutton lights.
2.	Connect Data Probe ground (⊥) lead to the ground of test. Leaving the Data Probe ground disconnected will result in inaccurate measurements.	

NOTE

Disregard blinking of GATE LED and Data Probe logic light.

3.	Place Data Probe tip on the circuit point at which peak plus or minus voltage is to be measured.	Display shows the peak voltage value at the Data Probe.

BLANK

APPENDIX 3: ACTUAL REPAIR OF P-C BOARDS.

This section gives information on touch-up, repairing and changing PCB's (printed-circuit boards) and is based on the information sheet 024 of the Centre for Technology of the Philips Company.

301. Required tools and materials.

It is recommended to equip a special work station where repairs and modifications on PCBs can be performed and where all tools and materials required will be available. Required are:

- magnifying glass to inspect soldering joints, holes etc
- solder sucking wick; this wick consists of copper litz impregnated in colophony resin. Because of the capillary action the heated solder is sucked up. The wick has a width of 1,6 mm. This size is available from Philips under the code number 0322 107 00091.
- soldering iron with suction, such as for instance the PACE brand, available locally. Recommended are the portable light duty model MP-1-E or the somewhat heavier type MBT-100-E for fixed installation.
- tweezers
- erase brush for mechanical cleaning
- temperature-controlled soldering iron of about 30 Watts with fine tip, for instance the type TCP 50 of Weller-Magnastat with tip No. 7.
- hand-held solder sucker,with as little recoil as possible
- side-cutting pliers
- suction soldering iron: a combination of a soldering iron with suction action with simply exchangeable hollow bit, temperature controlled heating, simple to clean. Such soldering irons are a.o. available from the brand PACE.
- isopropyl alcohol for cleaning the surface.
- adhesive glue, non conductive.

302. Bonding parts of the printed wiring which have become loose.

Sometimes the printed wiring can become loose and detach itself from the carrier board. To repair, proceed as follows:

1. Clean the conductor with alcohol and a brush.
2. Use the brush to apply a limited quantity of adhesive onto the conductor and around it for a distance of at least 3,5 mm.
3. Press the conductor home with a rod
4. Dry the PCB

303. Destructive Replacement of defective components.

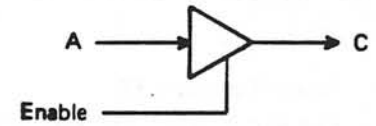
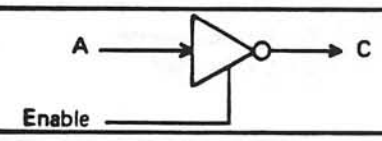
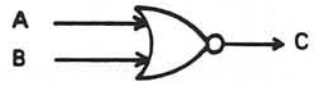
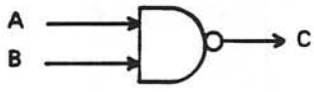
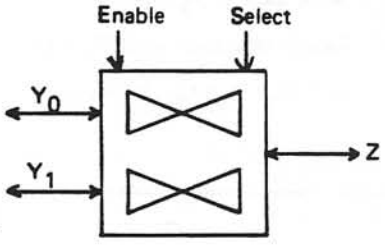
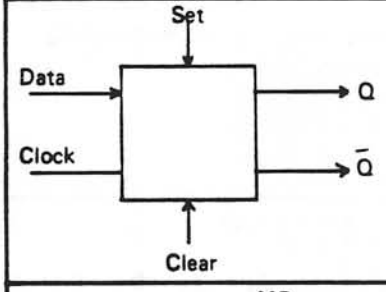
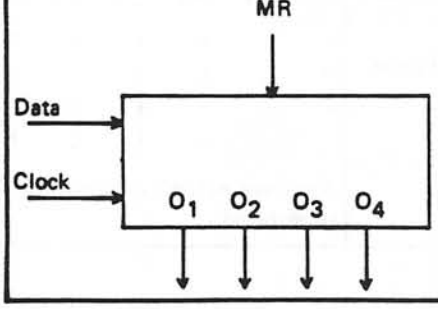
1. Cut the connecting wires on the component side.
2. Remove the remaining wires out of the holes by means of temperature controlled soldering iron and fine-point tweezers. Remove the solder out of the hole by means of the suction soldering iron or a simple soldering iron, solder sucker and sucking wick.
3. Check with the magnifying glass that the holes are completely empty; if necessary apply the soldering iron and sucking wick again.
4. Put the replacement I.C. into the place just cleaned, observing the polarity of the I.C.
5. Carefully solder the I.C. into place, taking care that all joints have "run" properly and that no short-circuits have been caused between two adjacent pins by applying too much solder.
6. Test the P.C.B. on the Exerciser.
7. Clean the spot and apply a thin coating of protective lacquer.

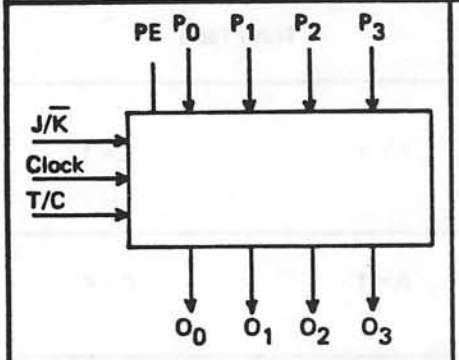
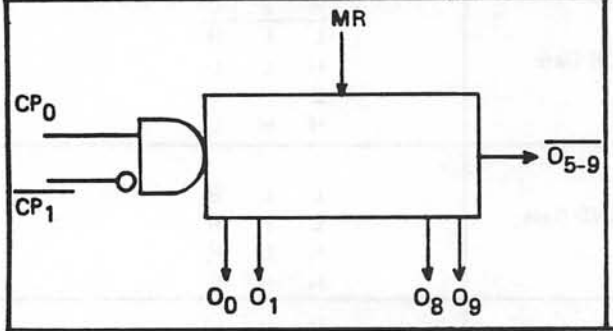
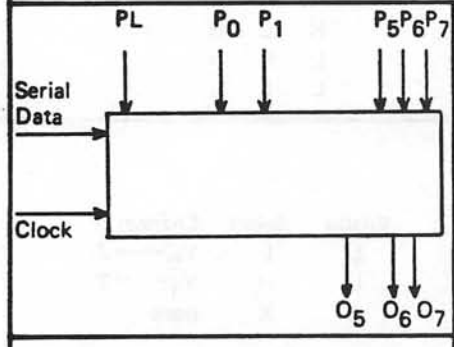
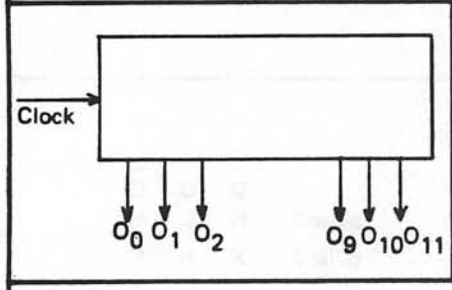
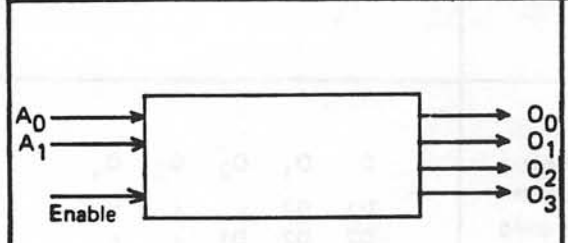
304. Non-destructive replacement of I.C.'s.

1. Remove all solder from the pins of the I.C. by means of a suction soldering iron or an iron + sucking wick.
2. Check with tweezers that all pins are loose.
3. Remove component.
4. Clean the mounting place of the I.C. with alcohol and a brush.
5. Place the I.C. into the holes just vacated , observing the correct polarity.
6. Solder the I.C. into place, using as little solder as possible, but making sure that the solder has "run" properly through the hole and correct contact is made.
7. Check the soldering spots with the aid of a magnifying glass on both sides, looking for "dry joints" and short circuits.
8. Check the P.C.B. on the Exerciser.
9. Clean the spot with alcohol and a brush and apply a coat of protective lacquer

305. Replacement of I.C.'s by soldering machines with standing wave.

When a workshop disposes of a wave soldering machine, it is possible to install a special nozzle on the wave, having the dimensions of the I.C., and melt the spot for about 3 seconds at the same time using an I.C. extractor to pull the I.C. from the P.C.B. Be careful not to burn the printed wiring by excessive heat!

Symbol	Name	Truth Table
	Buffer	A = 1 C = 1
	Inverting Buffer	A = 1 C = Ø
	NOR Gate	A B C L L H H L L L H L H H L
	NAND Gate	L L H L H H H L H H H L
	Exclusive-OR Gate	H H L H L H L H H L L L
	2-Channel Analogue Multiplexer	Enable Select Channel L L $Y_0 \longleftrightarrow Z$ L H $Y_1 \longleftrightarrow Z$ H X none
	Delay Type Flip Flop	D Q $\bar{Q}$ pulse 1 H L H pulse 2 X H L
	4-Bit Static Shift Register (positive going clock)	D O_1 O_2 O_3 O_4 D1 D2 x x x D2 D2 D1 x x D3 D3 D2 D1 x D4 D4 D3 D2 D1

Symbol	Name	Truth Table
	4-Bit Universal Shift Register (positive going clock)	Serial Operation: PE = L J$\overline{K}$ O_0 . . . . . . Parallel Operation: PE = H $P_0 = O_0$; . . . . . $P_3 = O_3$ T/C = H = non inverted T/C = L = inverted
	5-Stage Johnson Counter	Advance by positive-going CP_0 or negative-going CP_1 10 outputs plus $O_{5\,..\,9}$
	8-Bit Static Shift Register (Positive-going clock)	Serial operation when PL = L Serial data to O_5, O_6, O_7 Parallel operation when PL = H $P_5 = O_5$; $P_6 = O_6$; $P_7 = O_7$
	12-Stage Binary Counter	Ripple counter on positive-going clock
	1 - of - 4 Decoder/Multiplexer	Active High : A_0 A_1 O_0 O_1 O_2 O_3 L L H L L L H L L H L L L H L L H L H H L L L H Also used Active Low (inverted truth table)

ANNEX
4

DATA ON INTEGRATED CIRCUITS

CONTENTS ANNEX B

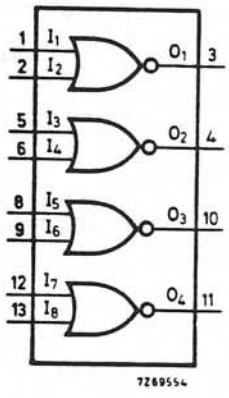
Annex B Data on Integrated circuits

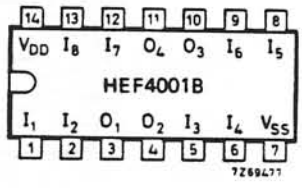
HEF4001B

gates

QUADRUPLE 2-INPUT NOR GATE

The HEF4001B provides the positive quadruple 2-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





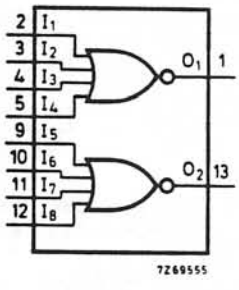
HEF4001BP: 14-lead DIL; plastic (SOT-27).
HEF4001BD: 14-lead DIL; ceramic (SOT-73).

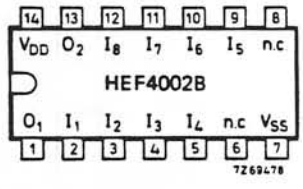
HEF4002B

gates

DUAL 4-INPUT NOR GATE

The HEF4002B provides the positive dual 4-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





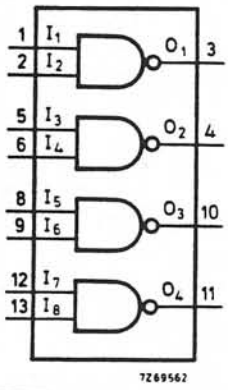
HEF4002BP : 14-lead DIL; plastic (SOT-27).
HEF4002BD : 14-lead DIL; ceramic (SOT-73).

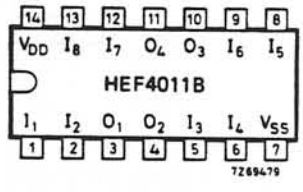
HEF4011B

gates

QUADRUPLE 2-INPUT NAND GATE

The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





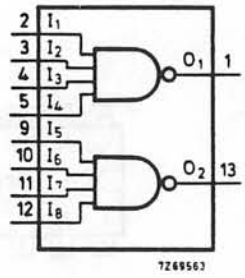
HEF4011BP : 14-lead DIL; plastic (SOT-27).
HEF4011BD: 14-lead DIL; ceramic (SOT-73).

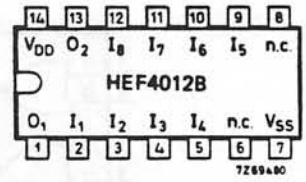
HEF4012B

gates

DUAL 4-INPUT NAND GATE

The HEF4012B provides the positive dual 4-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





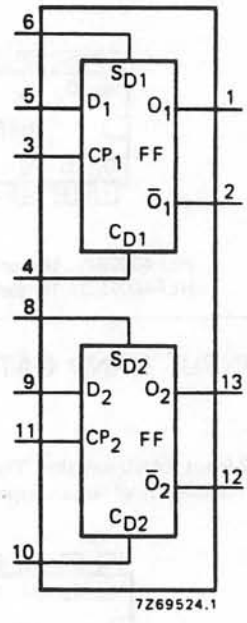
HEF4012BP: 14-lead DIL; plastic (SOT-27).
HEF4012BD: 14-lead DIL; ceramic (SOT-73).

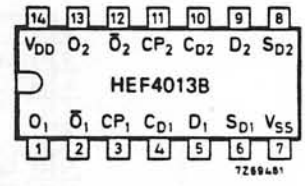
HEF4013B

flip-flops

DUAL D-TYPE FLIP-FLOP

The HEF4013B is a dual D-type flip-flop which is edge-triggered and features independent set direct, clear direct, and clock inputs. Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock.
The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance.





HEF4013BP: 14-lead DIL; plastic (SOT–27).
HEF4013BD: 14-lead DIL; ceramic (SOT–73).

TRUTH TABLES

inputs				outputs	
S_D	C_D	CP	D	O	$\bar{O}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

inputs				outputs	
S_D	C_D	CP	D	O_{n+1}	$\bar{O}_{n+1}$
L	L	∫	L	L	H
L	L	∫	H	H	L

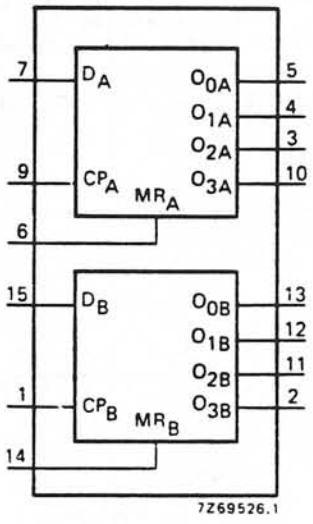
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transition

PINNING

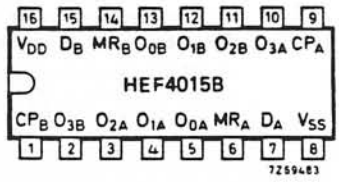
D data inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\bar{O}$ complement output

DUAL 4-BIT STATIC SHIFT REGISTER

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (O_0 to O_3) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces O_0 to O_3 to LOW, independent of CP and D.



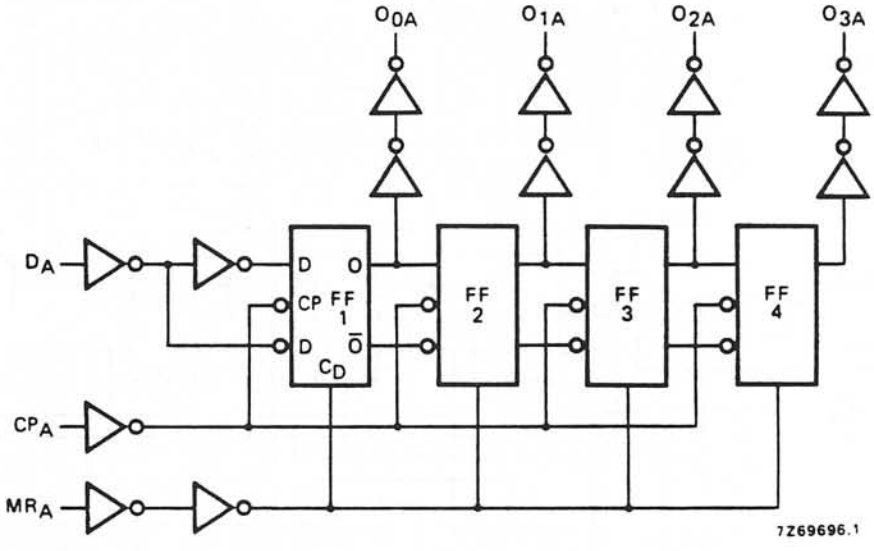
LOGIC DIAGRAM (one register)



HEF4015BP: 16-lead DIL; plastic (SOT-38Z).
HEF4015BD: 16-lead DIL; ceramic (SOT-74).

PINNING

D_A, D_B	serial data input
MR_A, MR_B	master reset input (active HIGH)
CP_A, CP_B	clock input (LOW-to-HIGH edge-triggered)
O_{0A}, O_{1A}, O_{2A}, O_{3A}	parallel outputs
O_{0B}, O_{1B}, O_{2B}, O_{3B}	parallel outputs



TRUTH TABLE

	inputs			outputs			
n	CP	D	MR	O_0	O_1	O_2	O_3
1	∫	D_1	L	D_1	X	X	X
2	∫	D_2	L	D_2	D_1	X	X
3	∫	D_3	L	D_3	D_2	D_1	X
4	⌝	D_4	L	D_4	D_3	D_2	D_1
	∫	X	L	no change			
	X	X	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

HEF4017B

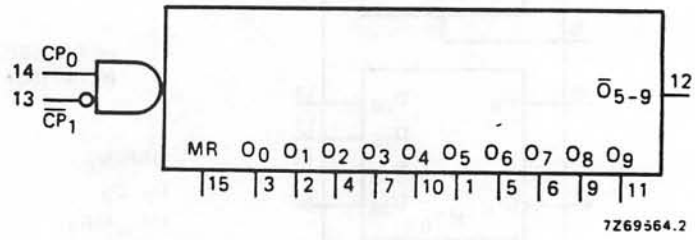
MSI

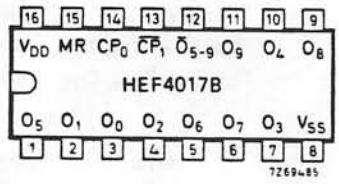
5-STAGE JOHNSON COUNTER

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop ($\overline{O}_{5-9}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also truth table on page 3).
When cascading counters, the $\overline{O}_{5-9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{5-9}$ = HIGH; O_1 to O_9 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).

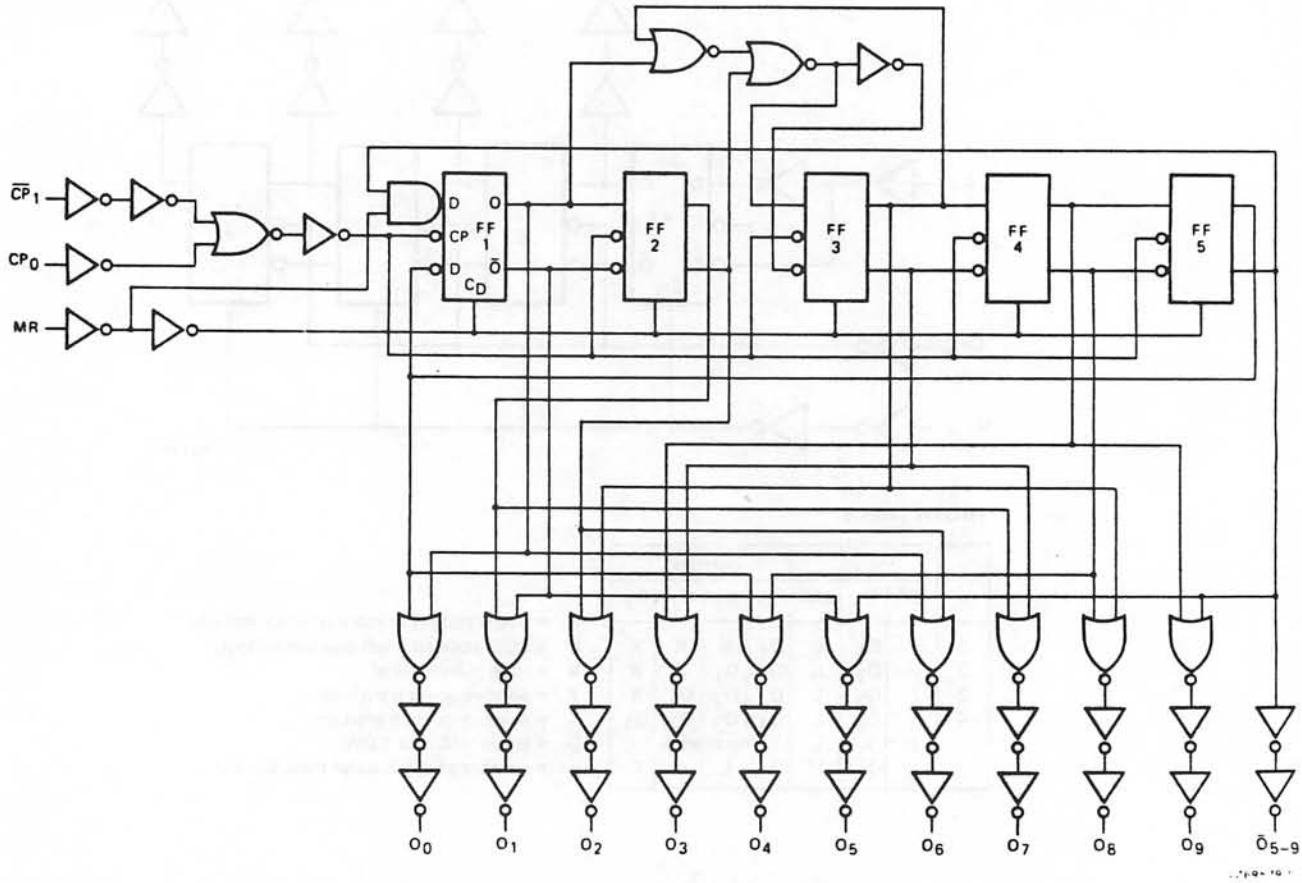




PINNING

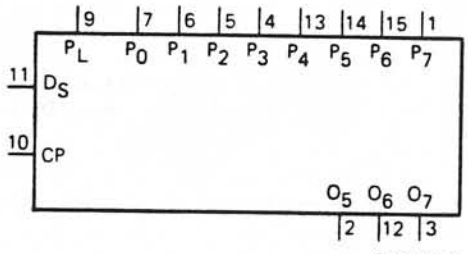
CP_0	clock input (LOW to HIGH triggered)
$\overline{CP}_1$	clock input (HIGH to LOW triggered)
MR	master reset input
O_0 to O_9	decoded outputs
$\overline{O}_{5-9}$	carry output (active LOW)

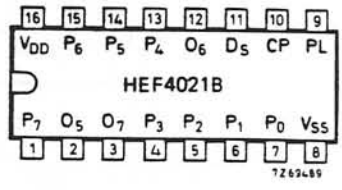
LOGIC DIAGRAM



8-BIT STATIC SHIFT REGISTER

The HEF4021B is an edge-triggered 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (D_S), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (P_0 to P_7) and buffered parallel outputs from the last three stages (O_5 to O_7). Information on P_0 to P_7 is asynchronously loaded into the register while PL is HIGH, independent of CP and D_S. When PL is LOW, data on D_S is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP.





HEF4021BP: 16-lead DIL; plastic (SOT-38Z).
HEF4021BD: 16-lead DIL; ceramic (SOT-74).

PINNING

PL	parallel load input
P_0 to P_7	parallel data inputs
D_S	serial data input
CP	clock input (LOW to HIGH edge-triggered)
O_5 to O_7	buffered parallel outputs from the last three stages

TRUTH TABLES

Serial operation

	inputs			outputs		
n	CP	D_S	PL	O_5	O_6	O_7
1	∫	D_1	L	X	X	X
2	∫	D_2	L	X	X	X
3	∫	D_3	L	X	X	X
6	∫	X	L	D_1	X	X
7	∫	X	L	D_2	D_1	X
8	∫	X	L	D_3	D_2	D_1
	⌝	X	L	no change		

Parallel operation

	inputs			outputs		
n	CP	D_S	PL	O_5	O_6	O_7
	X	X	H	P_5	P_6	P_7

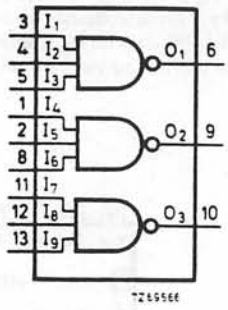
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

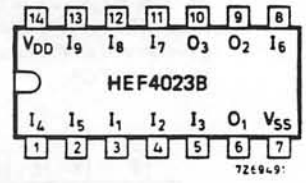
HEF4023B

gates

TRIPLE 3-INPUT NAND GATE

The HEF4023B provides the positive triple 3-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





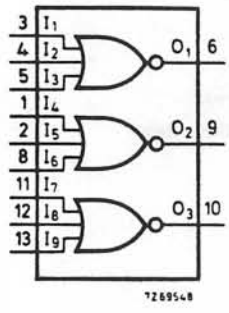
HEF4023BP : 14-lead DIL; plastic (SOT-27).
HEF4023BD : 14-lead DIL; ceramic (SOT-73).

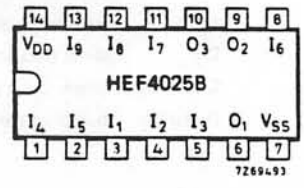
HEF4025B

gates

TRIPLE 3-INPUT NOR GATE

The HEF4025B provides the positive triple 3-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





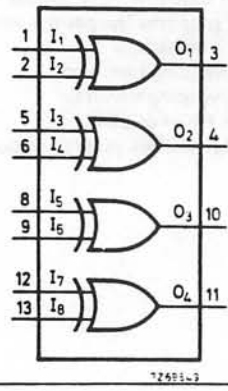
HEF4025BP : 14-lead DIL; plastic (SOT-27).
HEF4025BD : 14-lead DIL; ceramic (SOT-73).

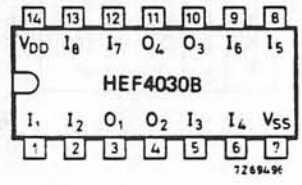
HEF4030B

gates

QUADRUPLE EXCLUSIVE-OR GATE

The HEF4030B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4030BP : 14-lead DIL; plastic (SOT-27).
HEF4030BD : 14-lead DIL; ceramic (SOT-73).

TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

4-BIT UNIVERSAL SHIFT REGISTER

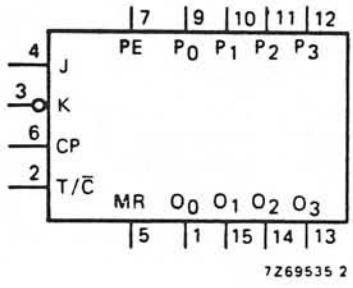
The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a true/complement input ($T/\overline{C}$) and an overriding asynchronous master reset input (MR).

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP.

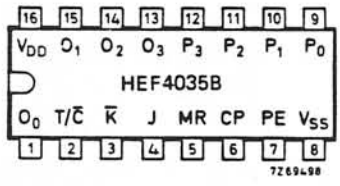
When PE is LOW, data is shifted into the first register position from J and $\overline{K}$ and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and $\overline{K}$.

The outputs (O_0 to O_3) are either inverting or non-inverting, depending on $T/\overline{C}$ state. With $T/\overline{C}$ HIGH, O_0 to O_3 are non-inverting (active HIGH) and when $T/\overline{C}$ is LOW, O_0 to O_3 are inverting (active LOW).

A HIGH on MR resets all four bit positions (O_0 to O_3 = LOW if $T/\overline{C}$ = HIGH, O_0 to O_3 = HIGH if $T/\overline{C}$ = LOW) independent of all other input conditions.



7Z69535 2



7Z69498

HEF4035BP: 16-lead DIL; plastic (SOT-38Z).
HEF4035BD: 16-lead DIL; ceramic (SOT-74).

PINNING

PE	parallel enable input
P_0 to P_3	parallel data inputs
J	first stage J-input (active HIGH)
$\overline{K}$	first stage K-input (active LOW)
CP	clock input (LOW to HIGH edge-triggered)
$T/\overline{C}$	true/complement input
MR	master reset input
O_0 to O_3	buffered parallel outputs

TRUTH TABLES

Serial operation

n	inputs				outputs			
	CP	J	$\overline{K}$	MR	O_0	O_1	O_2	O_3
1	∫	L	L	L	L	X	X	X
2	∫	H	H	L	H	L	X	X
3	∫	H	L	L	L	H	L	X
4	∫	H	L	L	H	L	H	L
5	∫	L	H	L	H	H	L	H
	⟍	X	X	L	no change			
	X	X	X	H	L	L	L	L

$T/\overline{C}$ = HIGH; PE = LOW

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

n = number of clock pulse transitions
∫ = positive-going transition
⟍ = negative-going transition

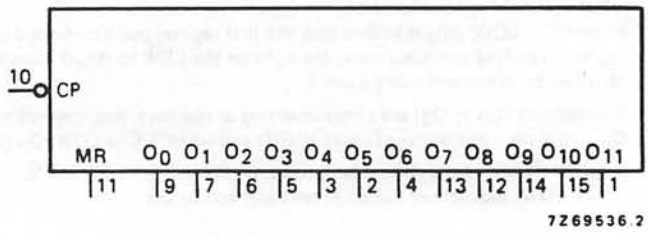
Parallel operation

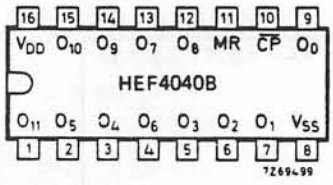
CP	inputs				outputs			
	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3
∫	H	H	H	H	H	H	H	H
∫	L	L	L	L	L	L	L	L

$T/\overline{C}$ = HIGH; PE = HIGH; MR = LOW

12-STAGE BINARY COUNTER

The HEF4040B is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 to O_{11}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$.



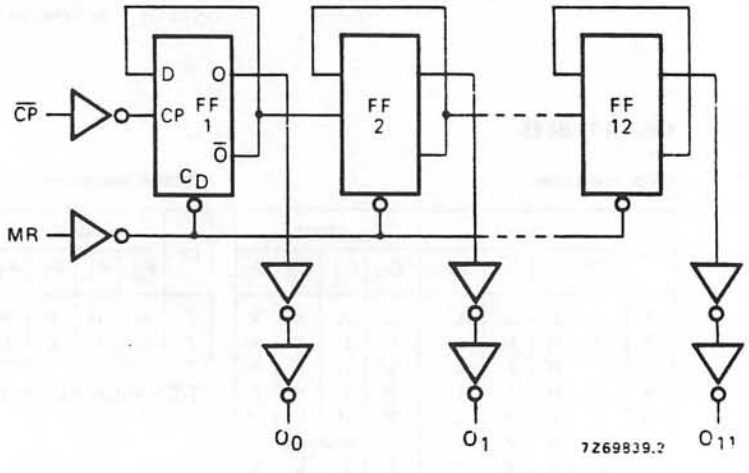


HEF4040BP: 16-lead DIL; plastic (SOT-38Z).
HEF4040BD: 16-lead DIL; ceramic (SOT-74).

PINNING

$\overline{CP}$	clock input (HIGH to LOW edge-triggered)
MR	master reset input (active HIGH)
O_0 to O_{11}	parallel outputs

LOGIC DIAGRAM



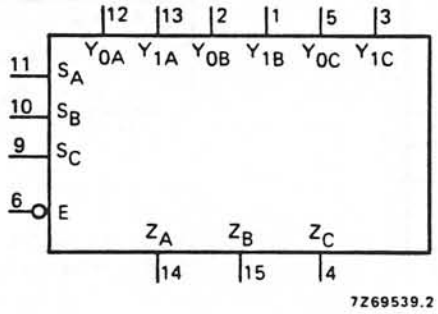
TRIPLE 2-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

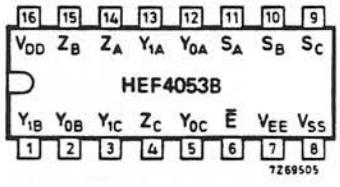
The HEF4053B is a triple 2-channel analogue multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (Y_0 and Y_1), a common input/output (Z), and select inputs (S_n). Each also contains two-bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_n. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_A to S_C.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and $\overline{E}$). Their voltage limits are the same as for all other digital LOCMOS. The analogue inputs/outputs (Y_0, Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).





PINNING

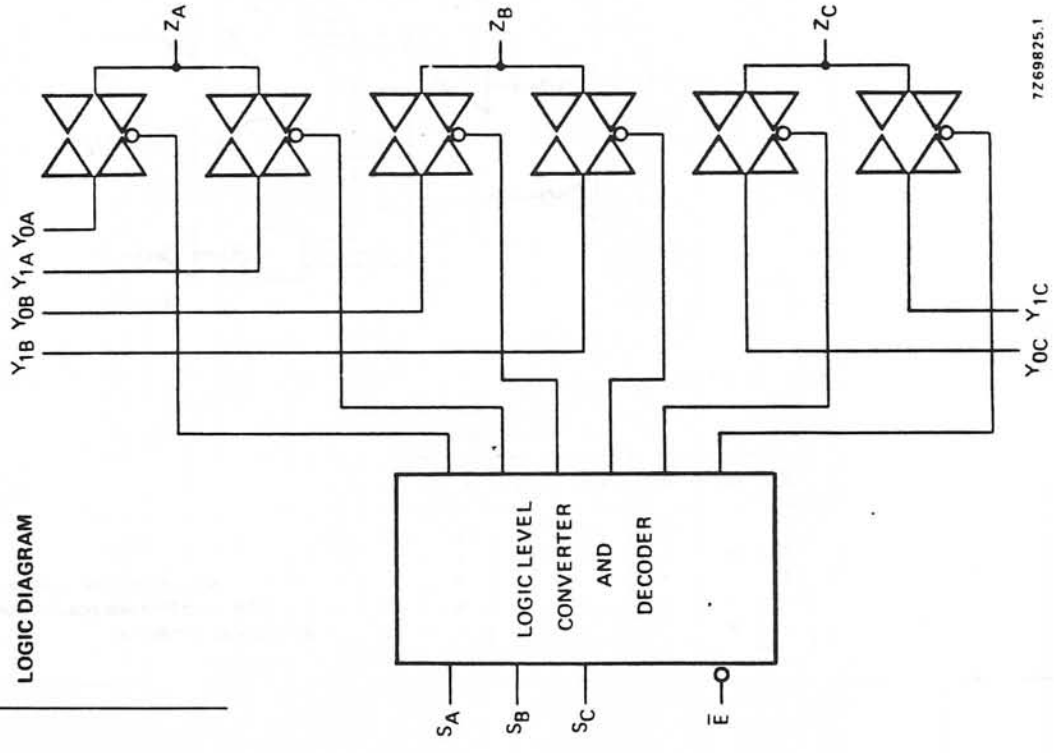
Y_{0A} to Y_{0C}	independent inputs/outputs
Y_{1A} to Y_{1C}	independent inputs/outputs
S_A to S_C	select inputs
$\overline{E}$	enable input (active LOW)
Z_A to Z_C	common inputs/outputs

FUNCTION TABLE

inputs		channel ON
$\overline{E}$	S_A	
L	L	Y_{0A}–Z_A
L	H	Y_{1A}–Z_A
H	X	none

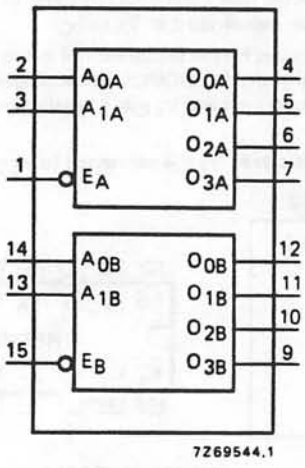
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

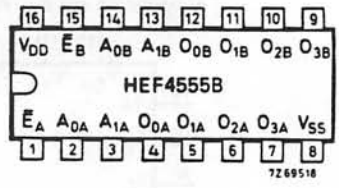
LOGIC DIAGRAM



DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4555B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active HIGH (O_0 to O_3). When used as a decoder, $\overline{E}$ when HIGH, forces O_0 to O_3 LOW. When used as a demultiplexer, the appropriate output is selected by the data on A_0 and A_1. All unselected outputs are LOW.



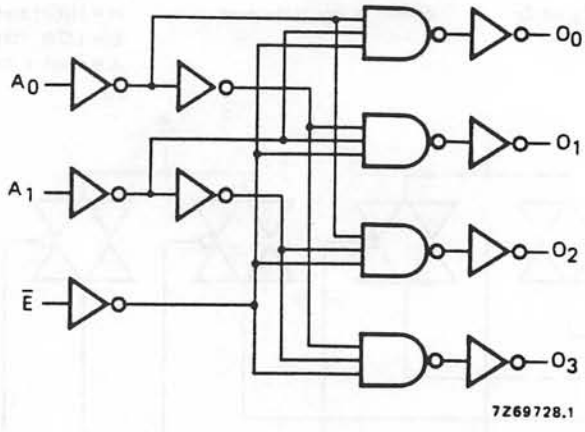


HEF4555BP: 16-lead DIL; plastic (SOT-38Z).
HEF4555BD: 16-lead DIL; ceramic (SOT-74).

PINNING

$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
O_0 to O_3	outputs (active HIGH)

LOGIC DIAGRAM



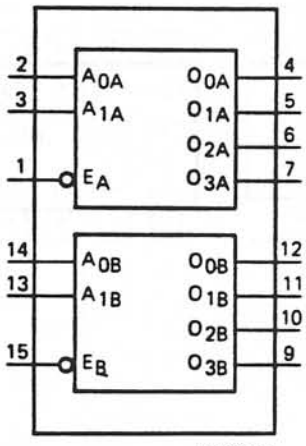
TRUTH TABLE

inputs			outputs			
$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4556B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active LOW (O_0 to O_3). When used as a decoder, $\overline{E}$ when HIGH, forces O_0 to O_3 HIGH. When used as a demultiplexer, the appropriate output is selected by the data on A_0 and A_1. All unselected outputs are HIGH.

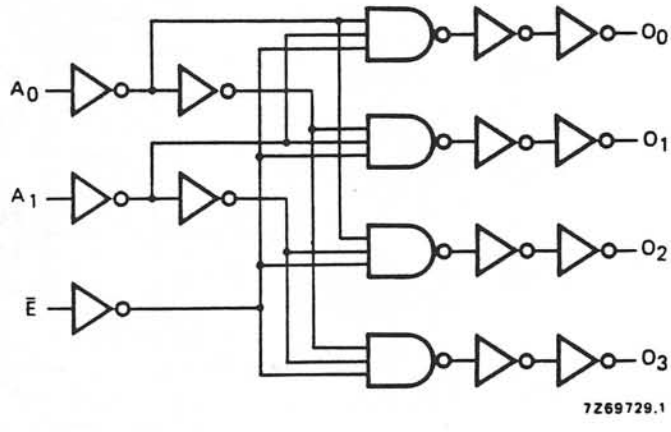


HEF4556BP: 16-lead DIL; plastic (SOT-38Z).
HEF4556BD: 16-lead DIL; ceramic (SOT-74).

PINNING

$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
O_0 to O_3	outputs (active LOW)

LOGIC DIAGRAM



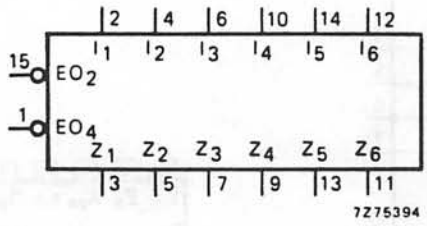
TRUTH TABLE

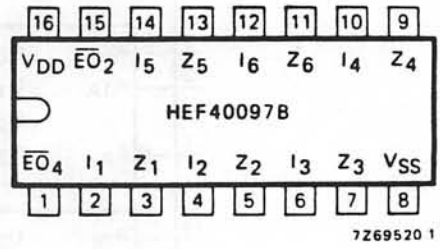
inputs			outputs			
$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

3-STATE HEX NON-INVERTING BUFFER

The HEF40097B is a hex non-inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions.

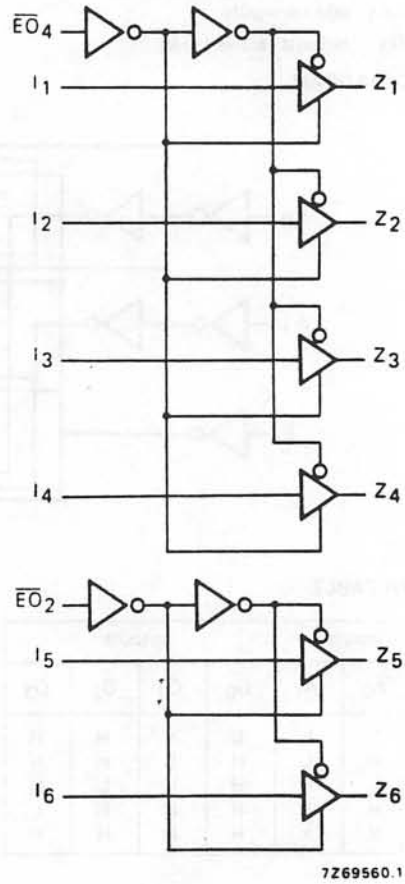




PINNING

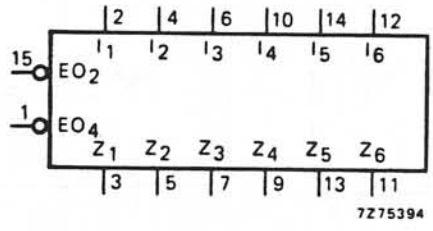
I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
Z_1 to Z_6	buffer outputs (active HIGH)

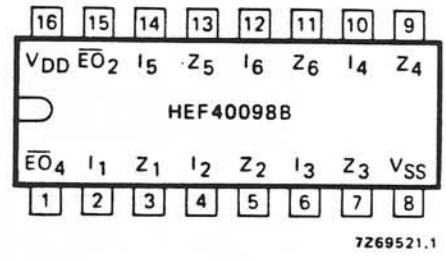
LOGIC DIAGRAM



3-STATE HEX INVERTING BUFFER

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state regardless of the other input conditions.

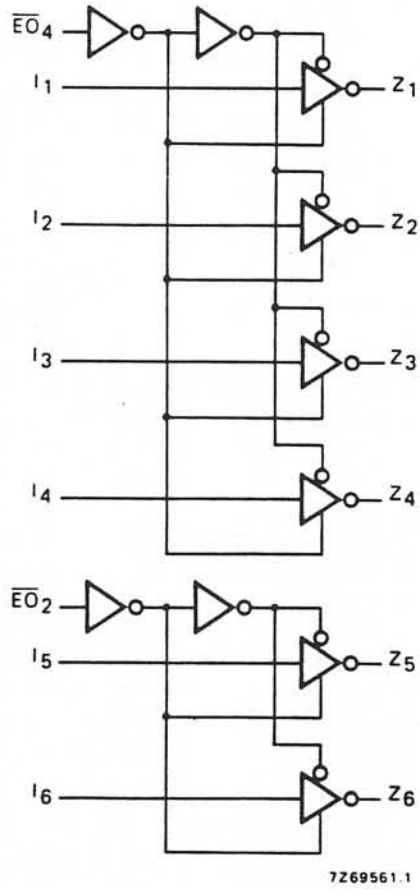




PINNING

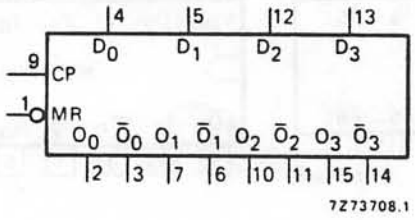
I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
Z_1 to Z_6	buffer outputs (active LOW)

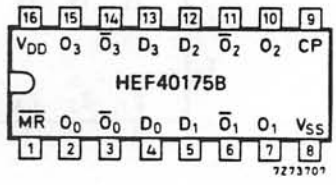
LOGIC DIAGRAM



QUADRUPLE D-TYPE FLIP-FLOP

The HEF40175B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), four buffered outputs (O_0 to O_3), and four complementary buffered outputs ($\overline{O}_0$ to $\overline{O}_3$). Information on D_0 to D_3 is transferred to O_0 to O_3 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_3 = LOW, $\overline{O}_0$ to $\overline{O}_3$ = HIGH), independent of CP and D_0 to D_3.



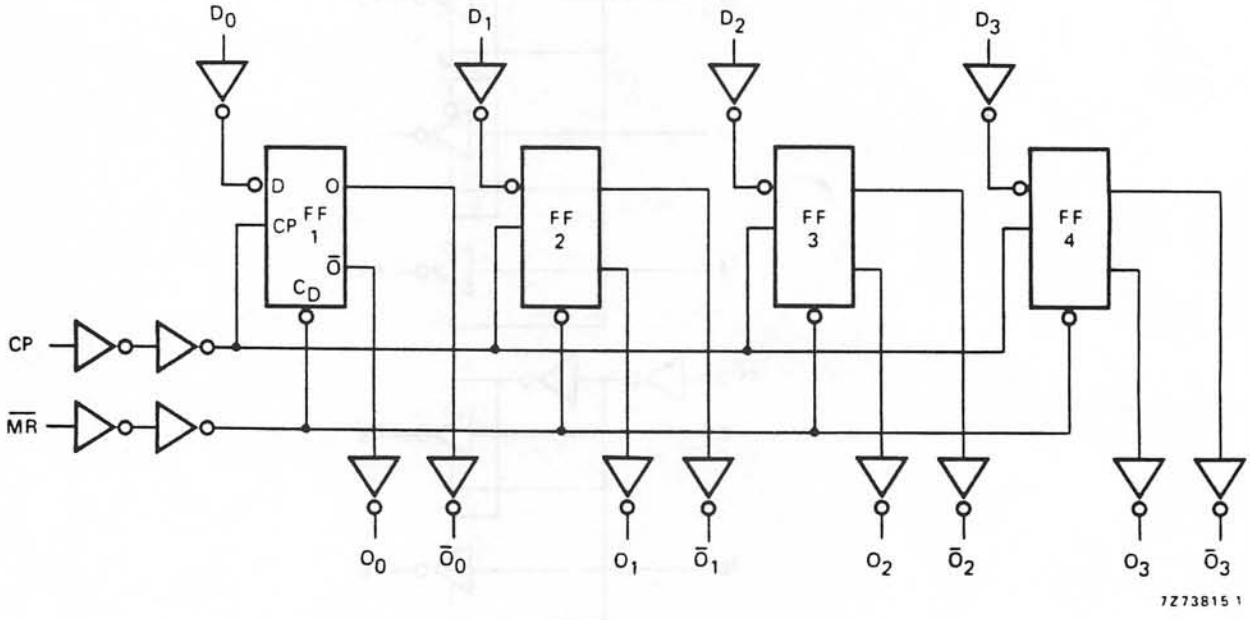


HEF40175BP: 16-lead DIL; plastic (SOT-38Z).
HEF40175BD: 16-lead DIL; ceramic (SOT-74).

PINNING

D_0 to D_3	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary buffered outputs

LOGIC DIAGRAM



54/7404
54H/74H04
54S/74S04
54LS/74LS04

ORDERING CODE (See Section 9 for further Package and Ordering Information.)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	Fig. A Fig. A	N7404N • N74H04N N74S04N • N74LS04N	
Ceramic DIP	Fig. A Fig. A	N7404F • N74H04F N74S04F • N74LS04F	S5404F • S54H04F S54S04F • S54LS04F
Flatpak	Fig. B Fig. A		S5404W • S54H04W S54S04W • S54LS04W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (See Note a)

PINS		54/74	54H/74H	54S/74S	54LS/74LS
Inputs	I_{IH} (μA) I_{IL} (mA)	40 −1.6	50 −2.0	50 −2.0	20 −0.36
Outputs	I_{OH} (μA) I_{OL} (mA)	−400 16	−500 20	−1000 20	−400 4/8[a]

PIN CONFIGURATIONS

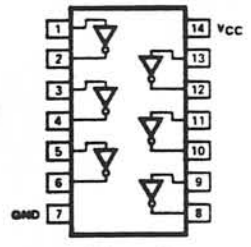


Figure A

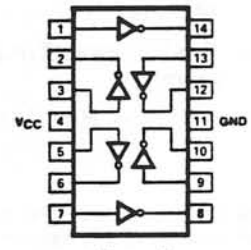


Figure B

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (See Note b)

PARAMETER,		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CCH}	Supply current	V_{CC} = Max, V_{IN} = 0V		12		26		24		2.5	mA
I_{CCL}	Supply current	V_{CC} = Max, V_{IN} ≥ 4.5V		33		58		54		6.6	mA

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions.)

PARAMETER		TEST CONDITIONS	54/74 C_L = 15 pF, R_L = 400 Ω		54H/74H C_L = 25 pF, R_L = 280 Ω		54S/74S C_L = 15 pF, R_L = 280 Ω		54LS/74LS C_L = 15 pF, R_L = 2k Ω		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		22		10		4.5		15	ns
t_{PHL}	Propagation delay	Waveform 1		15		10		5.0		15	ns

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial

2708
8K (1K x 8) UV ERASABLE PROM

	Max. Power	Max. Access
2708	800mW	450ns
2708L	425mW	450ns
2708-1	800mW	350ns
2708-6	800mW	550ns

- **Low Power Dissipation — 425 mW Max. (2708L)**
- **Fast Access Time — 350 ns Max. (2708-1)**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible during both Read and Program Modes**
- **Three-State Outputs — OR-Tie Capability**

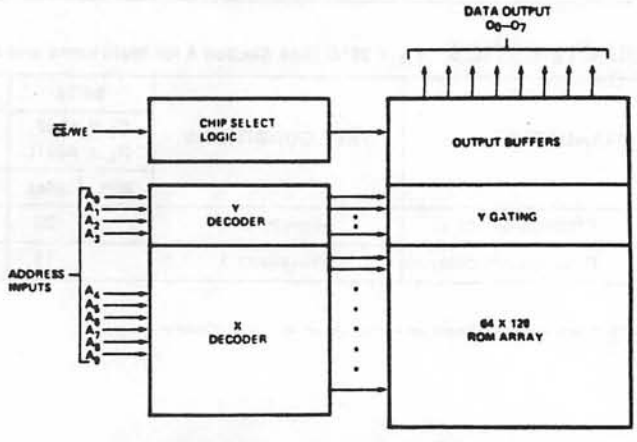
The Intel® 2708 is an 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures.

The 2708L at 425mW is available for systems requiring lower power dissipation than from the 2708. A power dissipation savings of over 50% without any sacrifice in speed is obtained with the 2708L. The 2708L has high input noise immunity and is specified at 10% power supply tolerance. A high-speed 2708-1 is also available at 350ns for microprocessors requiring fast access times.

The 2708 family is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

PIN CONFIGURATION

BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 25V	+12	V_{IHW}	-5	+5

2104A FAMILY
4096 x 1 BIT DYNAMIC RAM

	2104A-1	2104A-2	2104A-3	2104A-4
Max. Access Time (ns)	150	200	250	300
Read, Write Cycle (ns)	320	375	375	425
Max. IDD (mA)	35	32	30	30

- **Highest Density 4K RAM Industry Standard 16 Pin Package**
- **Low Power 4K RAM: 462mW Operating 27mW Standby**
- **All Inputs Including Clocks TTL Compatible**
- **±10% Tolerance on All Power Supplies +12V, +5V, -5V**
- **Refresh Period: 2 ms**
- **On-Chip Latches for Addresses, Chip Select and Data In**
- **Simple Memory Expansion: Chip Select**
- **Output is Three-State, TTL Compatible; Data is Latched and Valid into Next Cycle**
- **$\overline{RAS}$-Only Refresh Operation**

The Intel® 2104A is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density.

The efficient design of the 2104A allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

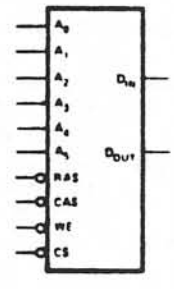
The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6 bit address words are latched into the 2104A by the two TTL clocks. Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

A new unique dynamic storage cell provides high speed along with low power dissipation and wide voltage margins. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a $\overline{RAS}$-only refresh cycle or read cycle at each of the 64 row addresses every 2 milliseconds.

The 2104A is designed for page mode operation, $\overline{RAS}$-only refresh, and $\overline{CAS}$-only deselect.

PIN CONFIGURATION

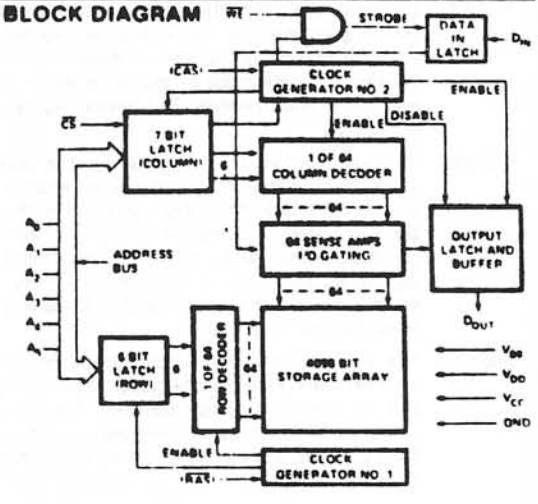
LOGIC DIAGRAM



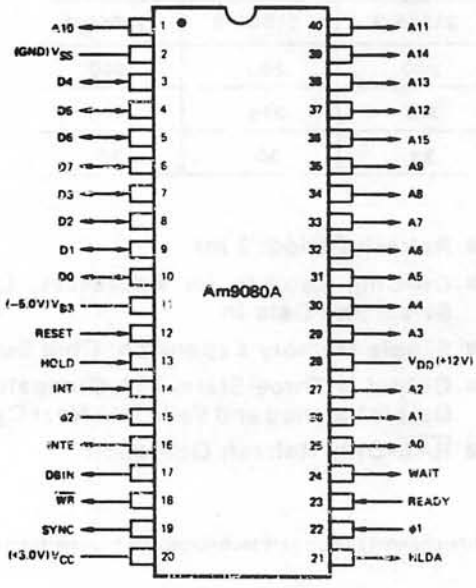
PIN NAMES

A_0-A_5	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

INTERFACE SIGNAL SUMMARY

TYPE	PINS	ABBREVIATION	SIGNAL
INPUT	1	V_{SS}	Ground
INPUT	3	V_{DD}, V_{CC}, V_{BB}	+12V, +5V, −5V Supplies
INPUT	2	$\phi 1$, $\phi 2$	Clocks
INPUT	1	RESET	Reset
INPUT	1	HOLD	Hold
INPUT	1	INT	Interrupt
INPUT	1	READY	Ready
IN/OUT	8	D_0–D_7	Data Bus
OUTPUT	16	A_0–A_{15}	Address
OUTPUT	1	INTE	Interrupt Enable
OUTPUT	1	DBIN	Data Bus In Control
OUTPUT	1	$\overline{WR}$	Write Not
OUTPUT	1	SYNC	Cycle Synchronization
OUTPUT	1	HLDA	Hold Acknowledge
OUTPUT	1	WAIT	Wait

INTERFACE SIGNAL DESCRIPTION

$\phi 1$, $\phi 2$ The Clock inputs provide basic timing generation for all internal operations. They are non-overlapping two phase, high level signals. All other inputs to the processor are TTL compatible.

RESET The Reset input initializes the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop and the hold acknowledge flip-flop. The Reset signal should be active for at least three clock periods. The general registers are not cleared.

HOLD The Hold input allows an external signal to cause the processor to relinquish control over the address lines and the data bus. When Hold goes active, the processor completes its current operation, activates the Hlda output, and puts the 3-state address and data lines into their high-impedance state. The Holding device can then utilize the address and data busses without interference.

READY The Ready input synchronizes the processor with external units. When Ready is absent, indicating the external operation is not complete, the processor will enter the Wait state. It will remain in the Wait state until the clock cycle following the appearance of Ready.

INT The Interrupt input signal provides a mechanism for external devices to modify the instruction flow of the program in progress. Interrupt requests are handled efficiently with the vectored interrupt procedure and the general purpose stack. Interrupt processing is described in more detail on the next page.

D_0–D_7 The Data Bus is comprised of 8 bidirectional signal lines for transferring data, instructions and status information between the processor and all external units.

A_0–A_{15} The Address Bus is comprised of 16 output signal lines used to address memory and peripheral devices.

SYNC The Sync output indicates the start of each processor cycle and the presence of processor status information on the data bus.

DBIN The Data Bus In output signal indicates that the bidirectional data bus is in the input mode and incoming data may be gated onto the Data Bus.

WAIT The Wait output indicates that the processor has entered the Wait state and is prepared to accept a Ready from the current external operation.

$\overline{WR}$ The Write output indicates the validity of output on the data bus during a write operation.

HLDA The Hold Acknowledge output signal is a response to a Hold input. It indicates that processor activity has been suspended and the Address and Data Bus signals will enter their high impedance state.

INTE The Interrupt Enable output signal shows the status of the interrupt enable flip-flop, indicating whether or not the processor will accept interrupts.

Am9208
1024 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 1024 x 8 organization
- High speed – 250ns access time
- Fully capacitive inputs – simplified driving
- 2 fully programmable chip selects – increased flexibility
- Logic voltage levels compatible to TTL
- Three-state output buffers – simplified expansion
- Standard supply voltages – +12V, +5.0V
- No V_{BB} supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Direct plug-in replacement for Intel 8308/2308 and T.I. 4700

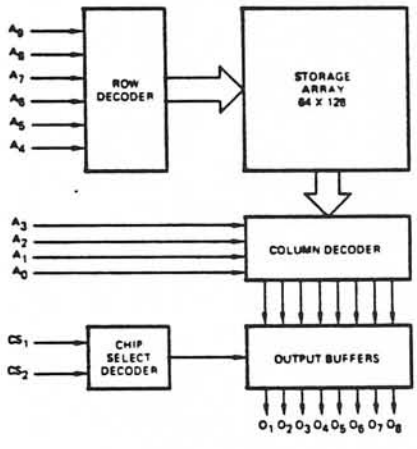
FUNCTIONAL DESCRIPTION

The Am9208 devices are high performance, 8192 bit, static, mask programmed, read only memories. Each memory is implemented as 1024 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 1024 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

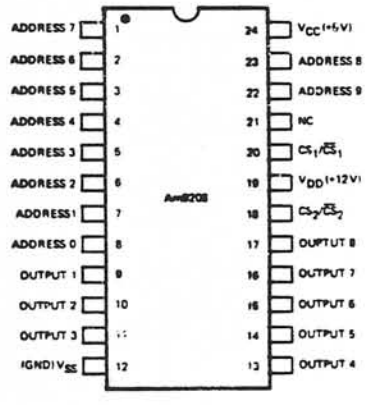
Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9208 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9208 is pin compatible with the Am9216 which is a 16k-bit mask programmed ROM. Input and output voltage levels are compatible to TTL specifications, providing simplified interfacing.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Access Time		
		400ns	300ns	250ns
Hermetic DIP	$0°C \leq T_A \leq 70°C$	Am9208BDC	Am9208CDC	Am9208DDC
	$-55°C \leq T_A \leq 125°C$	Am9208BDM	Am9208CDM	

BLANK

Am9080A
8-Bit Microprocessor

Distinctive Characteristics

- Plug-in replacements for 8080A, 8080A-1, 8080A-2
- High-speed version with 1μsec instruction cycle
- Military temperature range operation to 1.5μsec
- Ion-implanted, n-channel, silicon-gate MOS technology
- 3.2mA of output drive at 0.4V (two full TTL loads)
- 700mV of high, 400mV of low level noise immunity
- 820mW maximum power dissipation at ±5% power
- 100% reliability assurance testing to MIL-STD-883

GENERAL DESCRIPTION

The Am9080A products are complete, general-purpose, single-chip digital processors. They are fixed instruction set, parallel, 8-bit units fabricated with Advanced N-Channel Silicon Gate MOS technology. When combined with external memory and peripheral devices, powerful microcomputer systems are formed. The Am9080A may be used to perform a wide variety of operations, ranging from complex arithmetic calculations to character handling to bit control. Several versions are available offering a range of performance options.

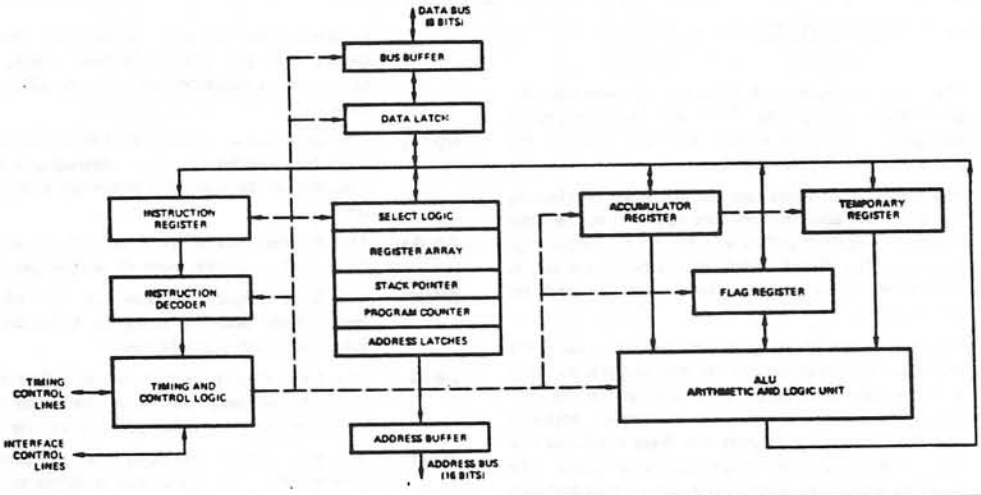
The processor has a 16-bit address bus that may be used to directly address up to 64K bytes of memory. The memory may be any combination of read/write and read-only. Data are transferred into or out of the processor on a bi-directional 8-bit data bus that is separate from the address lines. The data bus transfers instructions, data and status information between system devices. All transfers are handled using asynchronous handshaking controls so that any speed memory or I/O device are easily accommodated.

An accumulator plus six general purpose registers are available to the programmer. The six registers are each 8 bits long and may be used singly or in pairs for both 8 and 16-bit operations. The accumulator forms the primary working register and is the destination for many of the arithmetic and logic operations.

A general purpose push-down stack is an important part of the processor architecture. The contents of the stack reside in R/W memory and the control logic, including a 16-bit stack pointer, is located on the processor chip. Subroutine call and return instructions automatically use the stack to store and retrieve the contents of the program counter. Push and Pop instructions allow direct use of the stack for storing operands, passing parameters and saving the machine state.

An asynchronous vectored interrupt capability is included to allow external signals to modify the instruction stream. The interrupting device may specify an interrupt instruction to be executed and may thus vector the program to a particular service location, or perform some other direct function. Direct memory access (DMA) capability is also included.

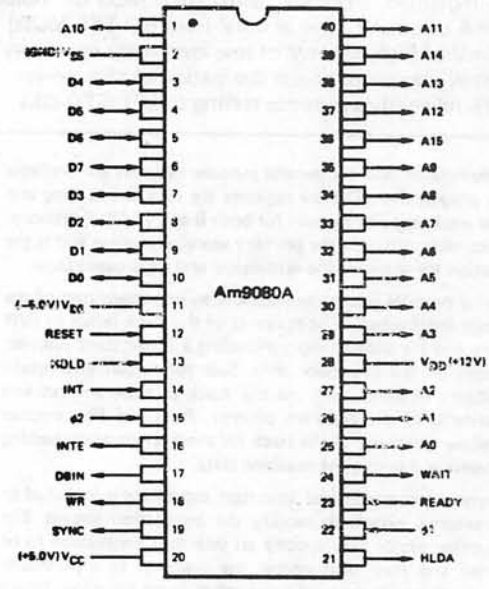
BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Clock Period			
		250 ns	320 ns	380 ns	480 ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	AM9080A-4DC	AM9080A-1DC C8080A-1	AM9080A-2DC C8080A-2	AM9080ADC C8080A
	$-55°C \leq T_A \leq +125°C$			AM9080A-2DM	AM9080ADM
Molded DIP	$0°C \leq T_A \leq +70°C$		AM9080A-1PC	AM9080A-2PC	AM9080APC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

INTERFACE SIGNAL SUMMARY

TYPE	PINS	ABBREVIATION	SIGNAL
INPUT	1	V_{SS}	Ground
INPUT	3	V_{DD}, V_{CC}, V_{BB}	+12V, +5V, –5V Supplies
INPUT	2	ϕ_1, ϕ_2	Clocks
INPUT	1	RESET	Reset
INPUT	1	HOLD	Hold
INPUT	1	INT	Interrupt
INPUT	1	READY	Ready
IN/OUT	8	D_0–D_7	Data Bus
OUTPUT	16	A_0–A_{15}	Address
OUTPUT	1	INTE	Interrupt Enable
OUTPUT	1	DBIN	Data Bus In Control
OUTPUT	1	$\overline{WR}$	Write Not
OUTPUT	1	SYNC	Cycle Synchronization
OUTPUT	1	HLDA	Hold Acknowledge
OUTPUT	1	WAIT	Wait

INTERFACE SIGNAL DESCRIPTION

ϕ_1, ϕ_2 The Clock inputs provide basic timing generation for all internal operations. They are non-overlapping two phase, high level signals. All other inputs to the processor are TTL compatible.

RESET The Reset input initializes the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop and the hold acknowledge flip-flop. The Reset signal should be active for at least three clock periods. The general registers are not cleared.

HOLD The Hold input allows an external signal to cause the processor to relinquish control over the address lines and the data bus. When Hold goes active, the processor completes its current operation, activates the Hlda output, and puts the 3-state address and data lines into their high-impedance state. The Holding device can then utilize the address and data busses without interference.

READY The Ready input synchronizes the processor with external units. When Ready is absent, indicating the external operation is not complete, the processor will enter the Wait state. It will remain in the Wait state until the clock cycle following the appearance of Ready.

INT The interrupt input signal provides a mechanism for external devices to modify the instruction flow of the program in progress. Interrupt requests are handled efficiently with the vectored interrupt procedure and the general purpose stack. Interrupt processing is described in more detail on the next page.

D_0–D_7 The Data Bus is comprised of 8 bidirectional signal lines for transferring data, instructions and status information between the processor and all external units.

A_0–A_{15} The Address Bus is comprised of 16 output signal lines used to address memory and peripheral devices.

SYNC The Sync output indicates the start of each processor cycle and the presence of processor status information on the data bus.

DBIN The Data Bus In output signal indicates that the bidirectional data bus is in the input mode and incoming data may be gated onto the Data Bus.

WAIT The Wait output indicates that the processor has entered the Wait state and is prepared to accept a Ready from the current external operation.

$\overline{WR}$ The Write output indicates the validity of output on the data bus during a write operation.

HLDA The Hold Acknowledge output signal is a response to a Hold input. It indicates that processor activity has been suspended and the Address and Data Bus signals will enter their high impedance state.

INTE The Interrupt Enable output signal shows the status of the interrupt enable flip-flop, indicating whether or not the processor will accept interrupts.

INSTRUCTION SET INTRODUCTION

The instructions executed by the Am9080A are variable length and may be one, two or three bytes long. The length is determined by the nature of the operation being performed and the addressing mode being used.

The instruction summary shows the number of successive memory bytes occupied by each instruction, the number of clock cycles required for the execution of the instruction, the binary coding of the first byte of each instruction, the mnemonic coding used by assemblers and a brief description of each operation. Some branch-type instructions have two execution times depending on whether the conditional branch is taken or not. Some fields in the binary code are labeled with alphabetic abbreviations. That shown as vvv is the address pointer used in the one-byte Call instruction (RST). Those shown as ddd or sss designate destination and source register fields that may be filled as follows:

111	A register
000	B register
001	C register
010	D register
011	E register
100	H register
101	L register
110	Memory

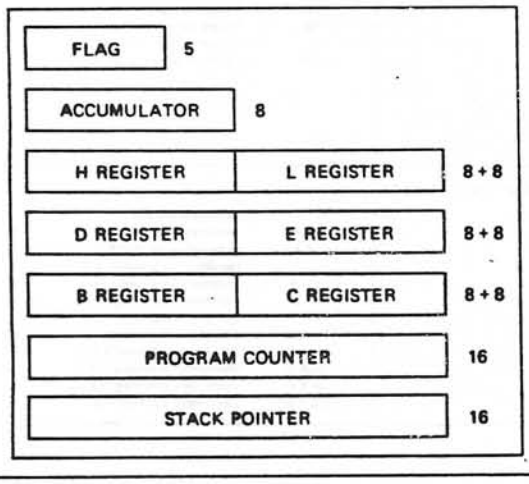
The register diagram shows the internal registers that are directly available to the programmer. The accumulator is the primary working register for the processor and is a specified or implied operand in many instructions. All I/O operations take place via the accumulator. Registers H, L, D, E, B and C may be used singly or in the indicated pairs. The H and L pair is the implied address pointer for many instructions.

The Flag register stores the program status bits used by the conditional branch instructions: carry, zero, sign and parity. The fifth flag bit is the intermediate carry bit. The flags and the accumulator can be stored on or retrieved from the stack with a single instruction. Bit positions in the flag register when pushed onto the stack (PUSH PSW) are:

7	6	5	4	3	2	1	0
S	Z	0	CY1	0	P	1	CY2

where S = sign, Z = zero, CY1 = intermediate carry, P = parity, CY2 = carry.

REGISTER DIAGRAM



During Sync time at the beginning of each instruction cycle the data bus contains operation status information that describes the machine cycle being executed. Positions for the status bits are:

7	6	5	4	3	2	1	0
MEMR	INP	M1	OUT	HLTA	STK	$\overline{WO}$	INTA

STATUS DEFINITION:

INTA	Interrupt Acknowledge. Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus when DBIN goes true.
$\overline{WO}$	Write or Output indicated when signal is low. When high, a Read or Input will occur.
STK	Stack indicates that the content of the stack pointer is on the address bus.
HLTA	Halt Acknowledge.
OUT	Output instruction is being executed.
M1	First instruction byte is being fetched.
INP	Input instruction is being executed.
MEMR	Memory Read operation.

INTERRUPT PROCESSING

When the processor interrupt mechanism is enabled (INTE=1), interrupt signals from external devices will be recognized unless the processor is in the Hold State. In handling an interrupt, the processor will complete the execution of the current instruction, disable further interrupts and respond with INTA status instead of executing the next sequential instruction in the interrupted program.

The interrupting device should supply an instruction opcode to the processor during the next DBIN time after INTA status appears.

Any opcode may be used except XTHL. If the instruction supplied is a single byte instruction, it will be executed. (The usual single byte instruction utilized is RST.) If the interrupt instruction is two or three bytes long, the next one or two processor cycles, as indicated by the DBIN signal, should be used by the external device to supply the succeeding byte(s) of the interrupt instruction. Note that INTA status from the processor is not present during these operations.

If the interrupt instruction is not some form of CALL, it is executed normally by the processor except that the Program Counter is not incremented. The next instruction in the interrupted program is then fetched and executed. Notice that the interrupt mechanism must be re-enabled by the processor before another interrupt can occur.

If the interrupt instruction is some form of CALL, it is executed normally. The Program Counter is stored and control transferred to the interrupt service subroutine. This routine has responsibility for saving and restoring the machine state and for re-enabling interrupts if desired. When the interrupt service is complete, a RETURN instruction will transfer control back to the interrupted program.

INSTRUCTION SET SUMMARY

Op Code [7][6][5][4][3][2][1][0]	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
DATA TRANSFER				
01dddsss	1	5	MOVr, r	Move register to register
01110sss	1	7	MOVm, r	Move register to memory
01ddd110	1	7	MOVr, m	Move memory to register
00ddd110	2	7	MVI, r	Move to register, immediate
00110110	2	10	MVI, m	Move to memory, immediate
00111010	3	13	LDA	Load Acc, direct
00001010	1	7	LDAX B	Load Acc, indirect via B & C
00011010	1	7	LDAX D	Load Acc, indirect via D & E
00101010	3	16	LHLD	Load H & L, direct
00100001	3	10	LXI H	Load H & L, immediate
00010001	3	10	LXI D	Load D & E, immediate
00000001	3	10	LXI B	Load B & C, immediate
00110001	3	10	LXI SP	Load stack pointer, immediate
00100010	3	16	SHLD	Store H & L, direct
00110010	3	13	STA	Store Acc, direct
00000010	1	7	STAX B	Store Acc, indirect via B & C
00010010	1	7	STAX D	Store Acc, indirect via D & E
11111001	1	5	SPHL	Transfer H & L to stack pointer
11101011	1	4	XCHG	Exchange D & E with H & L
11100011	1	18	XTHL	Exchange top of stack with H & L
11011011	2	10	IN	Input to Acc
11010011	2	10	OUT	Output from Acc
CONTROL				
01110110	1	7	HLT	Halt and enter wait state
00110111	1	4	STC	Set carry flag
00111111	1	4	CMC	Complement carry flag
11111011	1	4	EI	Enable interrupts
11110011	1	4	DI	Disable interrupts
00000000	1	4	NOP	No operation
BRANCHING				
11000011	3	10	JMP	Jump unconditionally
11011010	3	10	JC	Jump on carry
11010010	3	10	JNC	Jump on no carry
11001010	3	10	JZ	Jump on zero
11000010	3	10	JNZ	Jump on not zero
11110010	3	10	JP	Jump on positive
11111010	3	10	JM	Jump on minus
11101010	3	10	JPE	Jump on parity even
11100010	3	10	JPO	Jump on parity odd
11001101	3	17	Call	Call unconditionally
11011100	3	17-11	CC	Call on carry
11010100	3	17-11	CNC	Call on no carry
11001100	3	17-11	CZ	Call on zero
11000100	3	17-11	CNZ	Call on not zero
11110100	3	17-11	CP	Call on positive
11111100	3	17-11	CM	Call on minus
11101100	3	17-11	CPE	Call on parity even
11100100	3	17-11	CPO	Call on parity odd
11001001	1	10	RET	Return unconditionally
11011000	1	11-5	RC	Return on carry
11010000	1	11-5	RNC	Return on no carry
11001000	1	11-5	RZ	Return on zero
11000000	1	11-5	RNZ	Return on not zero
11110000	1	11-5	RP	Return on positive
11111000	1	11-5	RM	Return on minus
11101000	1	11-5	RPE	Return on parity even
11100000	1	11-5	RPO	Return on parity odd
11101001	1	5	PCHL	Jump unconditionally, indirect via H & L
11VVV111	1	11	RST	Restart

Op Code [7][6][5][4][3][2][1][0]	No. of Bytes	Clock Cycles	Assembly Mnemonic	Instruction Description
ARITHMETIC				
10000sss	1	4	ADDr	Add register to Acc
10001sss	1	4	ADCr	Add with carry register to Acc
10000110	1	7	ADDm	Add memory to Acc
10001110	1	7	ADCm	Add with carry memory to Acc
11000110	2	7	ADI	Add to Acc, immediate
11001110	2	7	ACI	Add with carry to Acc, immediate
00001001	1	10	DAD B	Double add B & C to H & L
00011001	1	10	DAD D	Double add D & E to H & L
00101001	1	10	DAD H	Double add H & L to H & L
00111001	1	10	DAD SP	Double add stack pointer to H & L
10010sss	1	4	SUBr	Subtract register from Acc
10011sss	1	4	SBBr	Subtract with borrow register from Acc
10010110	1	7	SUBm	Subtract memory from Acc
10011110	1	7	SBBm	Subtract with borrow memory from Acc
11010110	2	7	SUI	Subtract from Acc, immediate
11011110	2	7	SBI	Subtract with borrow from Acc, immediate
00100111	1	4	DAA	Decimal adjust Acc
STACK OPERATIONS				
11000101	1	11	PUSH B	Push registers B & C on stack
11010101	1	11	PUSH D	Push registers D & E on stack
11100101	1	11	PUSH H	Push registers H & L on stack
11110101	1	11	PUSH PSW	Push Acc and flags on stack
11000001	1	10	POP B	Pop registers B & C off stack
11010001	1	10	POP D	Pop registers D & E off stack
11100001	1	10	POP H	Pop registers H & L off stack
11110001	1	10	POP PSW	Pop Acc and flags off stack
LOGICAL				
10100sss	1	4	ANA r	And register with Acc
10100110	1	7	ANA m	And memory with Acc
11100110	2	7	ANI	And with Acc, immediate
10101sss	1	4	XRA r	Exclusive or register with Acc
10101110	1	7	XRA m	Exclusive Or memory with Acc
11101110	2	7	XRI	Exclusive Or with Acc, immediate
10110sss	1	4	ORA r	Inclusive Or register with Acc
10110110	1	7	ORA m	Inclusive Or memory with Acc
11110110	2	7	ORI	Inclusive Or with Acc, immediate
10111sss	1	4	CMP r	Compare register with Acc
10111110	1	7	CMP m	Compare memory with Acc
11111110	2	7	CPI	Compare with Acc, immediate
00101111	1	4	CMA	Compliment Acc
00000111	1	4	RLC	Rotate Acc left
00001111	1	4	RRC	Rotate Acc right
00010111	1	4	RAL	Rotate Acc left through carry
00011111	1	4	RAR	Rotate Acc right through carry
INCREMENT/DECREMENT				
00ddd100	1	5	INR r	Increment register
00110100	1	10	INR m	Increment memory
00000011	1	5	INX B	Increment extended B & C
00010011	1	5	INX D	Increment extended D & E
00100011	1	5	INX H	Increment extended H & L
00110011	1	5	INX SP	Increment stack pointer
00ddd101	1	5	DCR r	Decrement register
00110101	1	10	DCR m	Decrement memory
00001011	1	5	DCX B	Decrement extended B & C
00011011	1	5	DCX D	Decrement extended D & E
00101011	1	5	DCX H	Decrement extended H & L
00111011	1	5	DCX SP	Decrement stack pointer

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
All Signal Voltages With Respect to V_{BB}	−0.3V to +20V
All Supply Voltages With Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.5W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	T_A	V_{DD}	V_{CC}	V_{BB}	V_{SS}
Am9080A-XDC C8080A-X	0°C to +70°C	+12V ±5%	+5.0V ±5%	−5.0V ±5%	0V
Am9080A-XDM	−55°C to +125°C	+12V ±10%	+5.0V ±10%	−5.0V ±10%	0V

No signal or supply voltage should ever be greater than 0.3V more negative than V_{BB}.

ELECTRICAL CHARACTERISTICS over operating range (note 1)

Parameters	Description	Test Conditions			C8080A-X Min.	C8080A-X Typ.	C8080A-X Max.	Am9080A-XDC Min.	Am9080A-XDC Typ.	Am9080A-XDC Max.	Am9080A-XDM Min.	Am9080A-XDM Typ.	Am9080A-XDM Max.	Units
V_{IL}	Input LOW Voltage				−1.0		0.8	−1.0		0.8	−1.0		0.8	Volts
V_{IH}	Input HIGH Voltage				3.3		$V_{CC}+1$	3.0		$V_{CC}+1$	3.0		$V_{CC}+1$	Volts
V_{ILC}	Input LOW Voltage, Clock				−1.0		0.8	−1.0		0.8	−1.0		0.8	Volts
V_{IHC}	Input HIGH Voltage, Clock				9.0		$V_{DD}+1$	9.0		$V_{DD}+1$	$V_{DD}-2$		$V_{DD}+1$	Volts
			Am9080A-4					$V_{DD}-2$		$V_{DD}+1$				
V_{OL}	Output LOW Voltage	I_{OL} = 3.2mA								0.40			0.40	Volts
		I_{OL} = 1.9mA					0.45							Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −200µA						3.7			3.7			Volts
		I_{OH} = −100µA			3.7									
$I_{DD(AV)}$	V_{DD} Supply Current, Average	Operating, Minimum Clock Period	Am9080A Am9080A-2 Am9080A-1	T_A = +25 C		40			30	45		30	50	mA
				T_A = 0 C			70		35	50		35	55	
				T_A = −55 C								45	70	
			Am9080A-4	T_A = +25 C					45	60				
				T_A = 0 C					55	70				
$I_{CC(AV)}$	V_{CC} Supply Current, Average	Operating, Minimum Clock Period	Am9080A Am9080A-2 Am9080A-1	T_A = +25 C		60			25	30		15	35	mA
				T_A = 0 C			80		20	35		20	40	
				T_A = −55 C								25	50	
			Am9080A-4	T_A = +25 C					35	50				
				T_A = 0 C					40	60				
$I_{BB(AV)}$	V_{BB} Supply Current, Average	Operating, Minimum Clock Period					1.0			1.0			1.0	mA
I_{IL}	Input Leakage Current	(Note 4)					±10			±10			±10	µA
I_{CL}	Clock Leakage Current	$V_{SS} \le V_O \le V_{DD}$					±10			±10			±10	µA
I_{DL}	Data Bus Current, Input Mode (Note 2)	$V_{IN} \le V_{SS}+0.8V$					−100			−100			−100	µA
		$V_{IN} \ge V_{SS}+0.8V$					−2.0			−2.0			−2.0	mA
I_{FL}	Address and Data Bus Leakage in OFF State	$V_{A/D} = V_{CC}$					10			10			10	µA
		$V_{A/D} = V_{SS}$					−100			−100			−100	µA

CAPACITANCE

f = 1.0MHz, Inputs = 0V, T_A = 25°C

$V_{DD} = V_{CC} = V_{SS} = 0V$, $V_{BB} = -5.0V$

Parameters	Description	Typ.	Max.	Units
C_ϕ	Clock Input Capacitance	12	20	pF
C_I	Input Capacitance	4.0	8.0	pF
C_O	Output Capacitance	8.0	15	pF
$C_{I/O}$	I/O Capacitance	10	18	pF

SWITCHING CHARACTERISTICS over operating range

Boldface numbers are 9080A specs which are exceeded.

Parameters	Description	Test Conditions	Am9080A-4 Min.	Am9080A-4 Max.	Am9080A-1 C8080A-1 Min.	Am9080A-1 C8080A-1 Max.	Am9080A-2 C8080A-2 Min.	Am9080A-2 C8080A-2 Max.	Am9080A C8080A Min.	Am9080A C8080A Max.	Units
t_{DA}	Clock $\phi 2$ to Address Out Delay	Load Capacitance = 100pF		125		150		175		200	ns
t_{DD}	Clock $\phi 2$ to Data Out Delay			140		180		200		220	ns
t_{DI}	Clock $\phi 2$ to Data Bus Input Mode Delay	(Note 5)		t_{DF}		t_{DF}		t_{DF}		t_{DF}	ns
t_{DS1}	Data In to Clock $\phi 1$ Set-up Time	Both t_{DS1} and t_{DS2} must be satisfied	10		10		20		30		ns
t_{DS2}	Data In to Clock $\phi 2$ Set-up Time		110		120		130		150		ns
t_{DC}	Clock to Control Output Delay	Load Capacitance = 50pF		100		110		120		120	ns
t_{RS}	Ready to Clock $\phi 2$ Set-up Time		80		90		90		120		ns
t_H	Clock $\phi 2$ to Control Signal Hold Time		0		0		0		0		ns
t_{IS}	Interrupt to Clock $\phi 2$ Set-up Time		90		100		100		120		ns
t_{HS}	Hold to Clock $\phi 2$ Set-up Time		120		120		120		140		ns
t_{IE}	Clock $\phi 2$ to INTE Delay	Load Capacitance = 50pF		100		200		200		200	ns
t_{FD}	Clock $\phi 2$ to Address/Data OFF Delay		100			120		120		120	ns
t_{DF}	Clock $\phi 2$ to DBIN Delay	Load Capacitance = 50pF	25	110	25	130	25	140	25	140	ns
t_{DH}	Clock $\phi 2$ to Data In Hold Time	(Note 5)	–	–	–	–	–	–	–	–	ns
t_{AW}	Address Valid to Write Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{DW}	Output Data Valid to Write Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{KA}	Address Valid to Write Increment	(Note 8)		90		110		130		140	ns
t_{KD}	Output Data Valid to Write Increment	(Note 8)		130		150		170		170	ns
t_{WA}	Write to Address Invalid Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{WD}	Write to Output Data Invalid Delay	(Note 8)	–	–	–	–	–	–	–	–	ns
t_{HF}	HLDA to Address/Data OFF Delay	(Note 9)	–	–	–	–	–	–	–	–	ns
t_{WF}	Write to Address/Data OFF Delay	(Note 9)	–	–	–	–	–	–	–	–	ns
t_{KH}	HLDA to Address/Data OFF Increment	(Note 9)		40		50		50		50	ns
t_{AH}	DBIN to Address Hold Time		0		–20		–20		–20		ns

Notes: 1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.

2. Pull-up devices are connected to the Data Bus lines when the input signal is high during DBIN time. When switching the input from HIGH-to-LOW a transient current must be absorbed by the driving device until the input reaches a LOW level.

3. Timing reference levels —
   Clocks: HIGH = 8.0V, LOW = 1.0V
   Inputs: HIGH = 3.3V, LOW = 0.8V
   Outputs: HIGH = 2.0V, LOW = 0.8V

4. Control inputs impress currents on the driving signal during HIGH-to-LOW transitions. Values shown are for logic high or logic low levels. Peak current during transition is as much as 1.0mA.

5. Bus contention cannot occur and data hold times are adequate when DBIN is used to enable Data In. t_{DH} is the smaller of 50ns or t_{DF}.

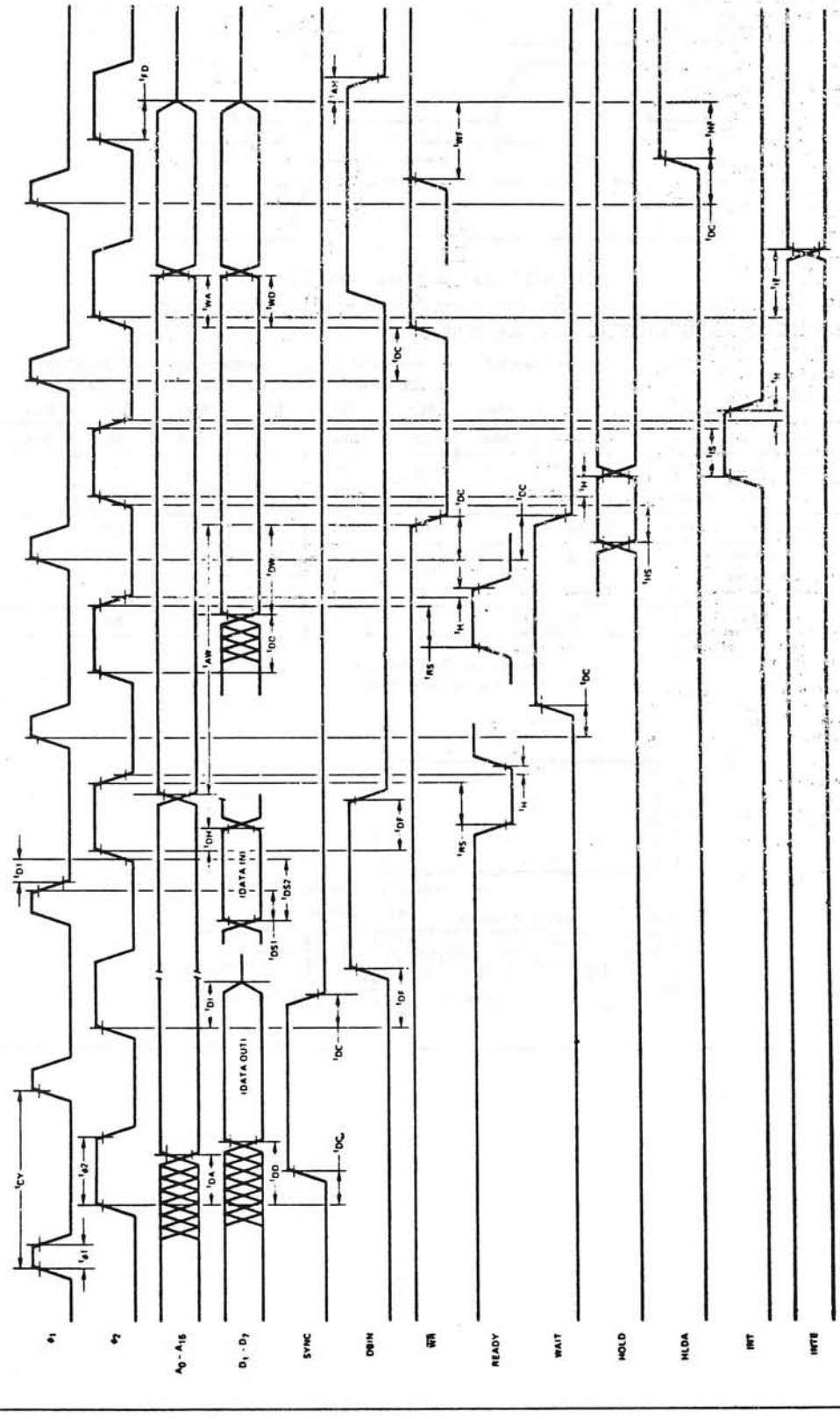
6. RESET should remain active for at least three clock periods.

7. With interrupts enabled, the interrupted instruction will be one with an interrupt input stable during the indicated interval of the last clock period of the preceeding instruction. Additional synchronization not necessary.

8. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi 2} - t_{KA}$
   $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - t_{KD}$
   For HLDA On: $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10ns$

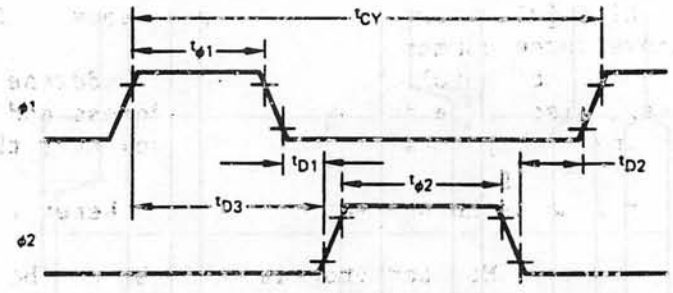
9. $t_{HF} = t_{D3} + t_{r\phi 2} - t_{KH}$
   $t_{WF} = t_{D3} + t_{r\phi 2} - 10ns$

SWITCHING WAVEFORMS SUMMARY



This chart presents relative timing waveform relationships and does not show actual processor operating cycles.

CLOCK WAVEFORM DETAIL

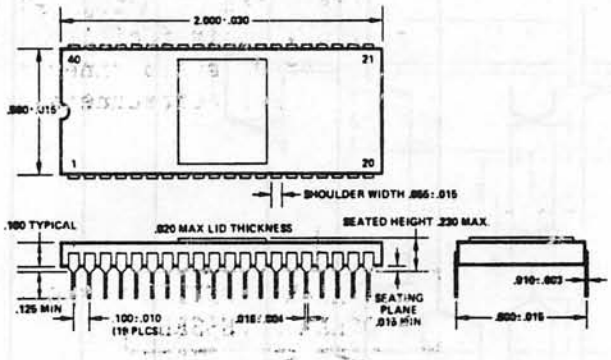


$t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1}$

CLOCK SWITCHING CHARACTERISTICS over operating range

Parameters	Description	Am9080A-4 Min.	Am9080A-4 Max.	Am9080A-1 C8080A-1 Min.	Am9080A-1 C8080A-1 Max.	Am9080A-2 C8080A-2 Min.	Am9080A-2 C8080A-2 Max.	Am9080A C8080A Min.	Am9080A C8080A Max.	Units
t_{CY}	Clock Period	250	2000	320	2000	380	2000	480	2000	ns
t_r, t_f	Clock Transition Times	0	15	0	25	0	50	0	50	ns
$t_{\phi1}$	Clock φ1 Pulse Width	50		50		60		60		ns
$t_{\phi2}$	Clock φ2 Pulse Width	120		145		175		220		ns
t_{D1}	φ1 to φ2 Offset	0		0		0		0		ns
t_{D2}	φ2 to φ1 Offset	50		60		70		70		ns
t_{D3}	φ1 to φ2 Delay	50		60		70		80		ns

PHYSICAL DIMENSIONS
40-Pin Hermetic DIP



APPENDIX 6: WRITING OF TEST PROGRAMS WITH THE EXERCISER.

601. Scope.

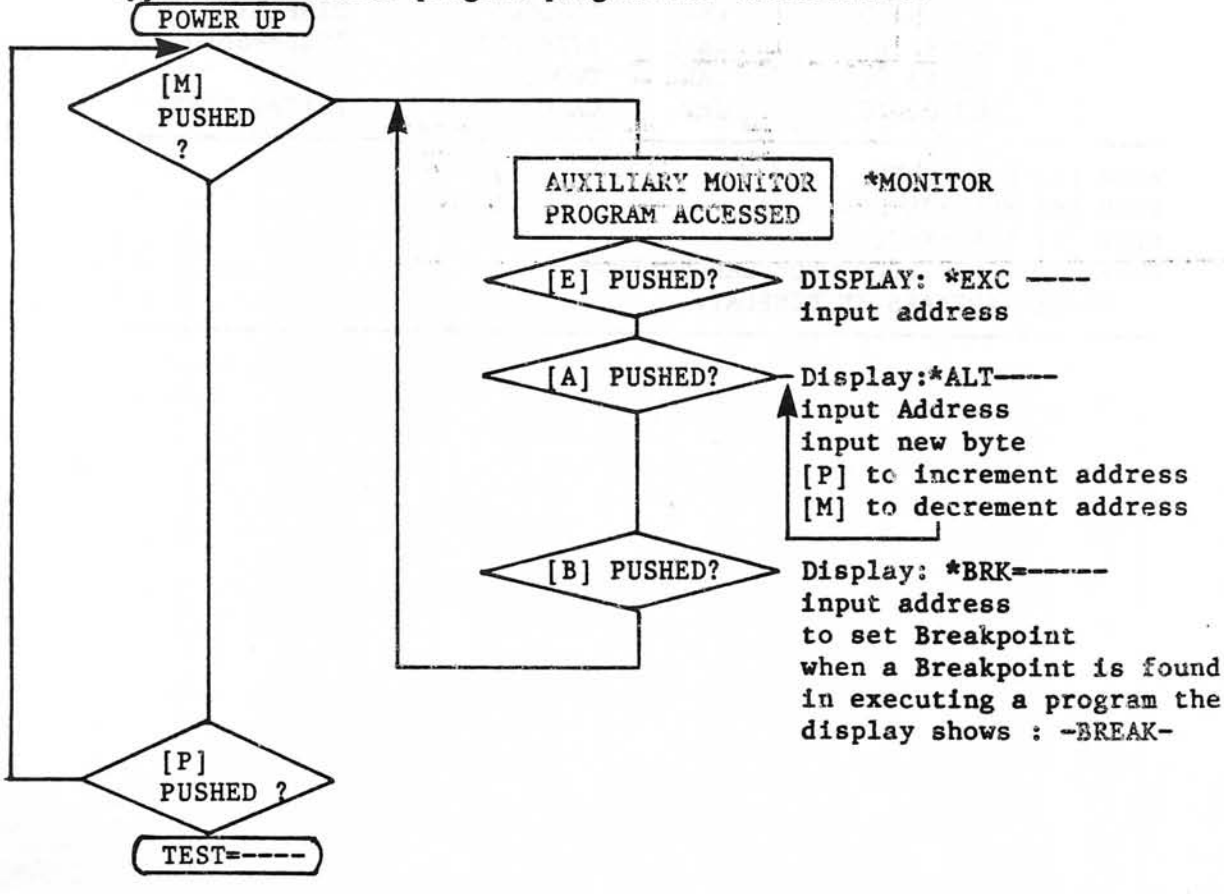
The exerciser is provided with a RAM and keyboard that can also be used to write test programs with the aid of the so-called Monitor program. As stated above, the Monitor program is accessed by pushing [M], whereupon the display shows *MONITOR. The Monitor knows three commands, viz:

[E] for Execute, to be followed by a 4-digit address
[A] for Alter, also to be followed by an address and
[B] for setting Breakpoints to retain control over the program during debugging.

The Exerciser remains in the set mode till a Reset is given [R].

The main use for the Monitor program would be to be able to execute additional programs which may be developed later and to calculate the checksums of ROMs of older types and the ROMs of the Key Manufacturing Program if incorporated; this is done by typing in the programs as listed below, giving a Reset and next typing in [M] for access to the Monitor, next typing in [A] for start address and the program itself, followed by [R] for Reset, [M] for access to Monitor and finally [E] followed by the start address to execute the typed-in program . The RAM in the Exerciser has space between 1000 and 15FF; for the remainder see the Memory Map in the listing of the Test Programs, section 12. The Instruction Set (OpCodes and Mnemonics) for programming the 8080 microprocessor are listed in Annex 4.

It is also possible to use the Exerciser to examine the data found at addresses in the crypto module itself (RAMs, ROMs and Input/Output addresses) in the [A] mode for Alter. In the alter mode, the address can be incremented by using [P] for Plus and decremented by using [M] for Minus. This facility can be used for gaining information on stored subroutines and checking a typed-in or stored program program for correctness.



602. CALCULATING THE CHECK SUM OF AN INDIVIDUAL ROM

The following program will calculate the checksum of a ROM:
PUSH [R] FOR RESET.
PUSH [M] FOR MONITOR.
PUSH [A] FOR ADDRESS.
ENTER STARTADDRESS: [1] [0] [0] [0].
ENTER CODES AS LISTED BELOW by typing : [0] [1] [P]
[F] [4] [P] etc.

```
   Addr:    CODE            Mnem
-----------------------------------------------------------------
CALC        1000   01 44 07        LXI     B,BUFF13
            CD 94 01          CALL    TEXT            "ROM=--"
INPUT       1004   CD 38 01         CALL    KEYS
            FE 00             CPI     '0'             INPUT NUMBER (1/8)
            CA 06 10          JZ      INPUT
            FE 09             CPI     '9'
            D2 06 10          JNC     INPUT
            C6 30             ADI     '30'H           "ROM= n"
            32 06 30          STA     (3006)
            F5                PUSH    PSW             SAVE n
            CD A3 01          CALL    TWOSEC          Delay
            01 34 07          LXI     B,BUFF1         Display
            CD 94 01          CALL    TEXT            "CSUM=--"
            F1                POP     AF              GET n
            D6 31             SUI     '31'H
            07                RLC
            07                RLC
            C6 80             ADI     '80'H
            67                MOV     H,A             GET BEGIN ADDRESS
            2E 00             MVI     L,0             IN 'HL'
            CD A0 06          CALL    TESTROM         CALCULATE CHECKSUM
            7B                MOV     A,E             GET CSUM
            11 06 30          LXI     D'3006'         DISPLAY
            CD B7 01          CALL    BYTE OUT        "CSUM=bb"
            CD A3 01          CALL    TWOSEC          DELAY
            C3 00 10          JMP     CALC            REPEAT TEST
-----------------------------------------------------------------
```

PUSH [X] FOR RESET
PUSH [M] FOR MONITOR
PUSH [E] FOR EXECUTE
ENTER ADDRESS "1000" FOR CALCULATION
RESULT APPEARS IN DISPLAY.

603. CALCULATE TOTAL CHECKSUM.

The following program will calculate the checksum of all ROMs on a Memory Board. There is a difference in the number of ROMs on a Board: there may be 7 or 8 ROMs mounted.

PUSH [R] FOR RESET
PUSH [M] FOR MONITOR
PUSH [A] FOR ADDRESS
ENTER [1] [1] [0] [0] FOR STARTADRESS
ENTER CODES AS LISTED BELOW BY TYPING: [2] [1] [P]
[0] [0] [P] etc.

```
      1100    21 00 80        LXI     H'8000'         BEGINADDRESS
              11 9C 00        LXI     D'9C00          END ADDRESS 7 ROMS
         or:  11 A0 00                  A000            END ADDRESS 8 ROMS
TOTAL
      1106    7E              MOV     A,M             CALC. CHECKSUM
              82              ADD     D
              57              MOV     D,A
              23              INX
              7C              MOV     A,H
              BB              CMP     E
              C2 06 11        JNZ     TOTAL
              D5              PUSH    D               SAVE CSUM
              01 E4 05        LXI     B BUFF 11       "CSUM=--"
              CD 94 01        CALL    TEXT
              D1              POP     D               GET CSUM
              7A              LVI     A,D
              11 06 30        LXI     D'3006'
              CD B7 01        CALL    BYTE OUT        "CSUM=DD"
              76
    HLT
```

PUSH [X] FOR RESET
PUSH [M] FOR MONITOR
PUSH [E] FOR EXECUTE
ENTER ADDRESS "1100" FOR CALCULATION
RESULT APPEARS IN DISPLAY.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