

DRAWINGS ATTACHED

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(54) GENERATOR PRODUCING A QUASI RANDOM
 SERIES OF ZEROES AND ONES

(71) We, NEDERLANDSE ORGANISATIE VOOR TOEGEPAST - NATUURWETENSCHAPPELIJK ONDERZOEK TEN BEHOEVE VAN DE RIJKSVERDEDIGING, a corporate body duly organised and existing under the laws of The Netherlands, of 22 Wassenaarseweg, The Hague, The Netherlands, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a generator producing a quasi random series of zeroes and ones ("0"s and "1"s), by which in this specification will be understood a circuit which, in accordance with the laws of probability allows the pulses of a periodically operating generator to appear at the output or not. A random series of "0"s and "1"s can also be described as a random series of pulses and no pulses. More generally the series could consist of a series of signals, which as a result of a process of drawing lots have one of two possible values.

For the purpose of the invention the circuit employs among other things a generator for periodical pulses, a noise source and a gate circuit. Dependent on the value of the noise voltage the pulses appear at the output or not.

In a circuit of this nature a requirement is to ensure that the probability for a pulse to appear at the output has a predetermined value.

With the present invention, the probability for a pulse to appear at the output is fixed at a predetermined or desired value, by continuously adding the pulses appearing at the output to the contents of a counter and by continuously subtracting a fraction of the pulses coming from the periodically operating pulse generator from the contents of the counter, the said fraction being equal

to the predetermined probability. A control voltage is derived from the value which represents the numerical contents of the counter, the control voltage being used to adjust the threshold level of the gate circuit controlled by the noise, at a rate of speed sufficiently low with respect to the repetition frequency of the pulses. The tendency of the adjustment is such that, if the average number of the pulses appearing at the output is too large, the control voltage tends to close the gate.

In order to avoid undesired correlation of pulses, the correlation in the noise voltage must fade out during the pulse period. In the present invention, the control voltage is derived from the most significant figures which, together with the remaining figures, form the number, which represents the contents of the counter, to avoid the correlation which could result from the controlling of the threshold level of the gate. Doing this, no adjustment of the threshold level of the gate circuit will take place, as long as, by adding the pulses appearing at the output to the contents and by subtracting the aforesaid fraction of the periodical pulses from the contents of the counter, the contents do not pass certain determined lower and upper limits in accordance with the division into most significant figures of the contents and less significant figures of the contents. These limits are hereinafter indicated as significance limits.

As a deviation of the probability of pulses appearing at the output ought to be detected by the determination of the number of pulses appearing at the output over a great number of pulse periods, the control voltage is led through a low pass filter, the time constant of which is large with respect to the pulse period.

In connection with the required possibility to handle series of ones and zeroes in which large numbers of only ones or only zeroes

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occur consecutively, it is necessary on the one hand to choose the counter capacity in accordance with this requirement, and on the other hand it is to be recommended to lay
5 the average value of the counter contents, calculated over a very long time, half-way along the range of the counter.

The significance limits lie symmetrically with respect to this point of adjustment.

10 The accompanying drawing is a circuit diagram explaining this invention. The arrangement illustrated in the drawing comprises a periodical pulse generator 1, a gate circuit 2, a counter 3 for adding and sub-
15 tracting pulses, a noise generator 4, a divider 5, an amplifier 6, a binary-numerical converter 7, a low pass filter 8, and adder circuit 9 for signals, and an output terminal 10 for the ones and the zeroes. The operation of the circuit is as follows.

If the output voltage of the amplifier 6 is high at the moment at which a pulse is fed to the gate by the pulse generator, a pulse appears at the output of the gate circuit 2.

25 If the output voltage of the amplifier 6 is low, no pulse will appear at the output of the gate circuit. The notions "high" and "low" will be illustrated later. The divider 5 determines the probability of a pulse
30 appearing at the output of the gate circuit by its division factor. If for instance the division factor is three, then the probability of pulses appearing at the output is one third. If the division factor should be 9/5
35 the chance of pulses appearing at the output would be 5/9.

In the counter 3, the pulses appearing at the output of the gate circuit are added to the contents and the pulses passed by the
40 divider are subtracted from the contents.

An adding and subtracting counter circuit may be formed by interlacing the time frames of pulses that are to be added and those that are to be subtracted, and by connect-
45 ing the counter as adder during the frame of the pulses to be added, and as subtractor during the frame of the pulses to be subtracted.

Switching occurs in a binary counter in
50 a way that will be explained below. The adding of "1" to the contents of a binary counter, consisting of triggers, means that the least significant trigger changes its state and that each trigger changes state, which
55 is preceded by less significant triggers in the "1" state at the moment in which the said "1" is fed to the counter. The "1" state of all less significant triggers is a necessary condition for the change of state of a trigger
60 when a "1" is added.

The subtracting of a "1" from the contents of a binary counter means that the least significant trigger changes its state and that each trigger changes state, which is
65 preceded by less significant triggers in the

"0" state at the moment in which the said "1" is fed to the counter. The "0" state of all less significant triggers is a necessary condition for the change of state of a trigger when a "1" is subtracted.

If each trigger can only change its state when a pulse is applied to it, an "And" gate may be used to control the admission of the pulse to the triggers.

For addition, it is necessary that a first
75 "And" gate be open only if all less significant triggers are in the "1" state.

For subtraction, it is necessary that a second "And" gate be open only if all less significant triggers are in the "0" state.

Each trigger, except the least significant one, has been supplied with a similar first
80 "And" gate and a similar second "And" gate, which may independently admit a pulse to the trigger.

A counter will add, when *all* the second
85 "And" gates have been blocked simultaneously, and will subtract when all the first "And" gates have been blocked simultaneously. The two "And" gate systems are connected to the complementary output terminals of a further trigger. The pulses of the pulse generator 1 are applied to the input terminals of this further trigger. This trigger changes its state at each pulse applied
95 to it.

The applied pulses are equally fed to circuit 2 if one trigger output terminal is high and are equally applied to circuit 5 if the other output terminal of the trigger
100 is high.

By doing this, two frames are obtained having the same repetition rates, which frames are time-interlaced.

The pulses of one frame are admitted to
105 the counter at a moment in which the first gate system has been deblocked. Similarly, the pulses of the other frame are admitted to the counter at a moment in which the second system has been deblocked.

The said trigger can at the same time command the switching of the counter 3, by blocking and de-blocking the "And" gate
110 systems.

The binary-numerical converter 7 can be
115 of the usual type having a resistance weighing network. By connecting the converter 7 only to the more significant triggers (e.g. five out of a total of ten) it is achieved that no variation occurs in the output voltage of
120 the converter, as long as the contents remain within the significance limits.

The low pass filter 8 can be an RC-combination having a sufficiently large time
125 constant.

The noise generator 4 is of a known type.

The circuit 9 combines the noise voltage and the output voltage of the low pass filter and feeds the combined voltage to the
130 amplifier 6.

The amplifier 6 is so designed that a minute variation of the input voltage will change the output voltage from the fixed value "high" to the fixed value "low". No great demands are made on the thermal stability of the amplifier, because the closed-circuit system can always find a state of equilibrium, by reacting to the "running away" of the amplifier with a shifting of the average value of the counter contents. In connection with what has been said about the significance limits, it is desirable that the thermal drift of the amplifier remains limited to a value which is such that the shifting of the value of the average counter contents required for its compensation comprises only a few units.

In connection with the possibility of the noise voltage of the noise generator 4, having a course which is such, determined by statistical laws, that a number of pulses appear or just fail to appear at the output, which number is so large that the counter contents reach the maximum or the minimum of the capacity, it is desirable to take steps to prevent the counter from being brought from its maximum position into its minimum position by one or more pulses, or vice versa. A measure suitable for this purpose in a binary counter is the provision of a diode gate circuit, the output of which becomes low and thereby blocks the supply of the pulses to be added, if the triggers of the counter indicate its maximum position, and providing a similar diode gate circuit, which blocks the supply of the pulses which are to be subtracted if the triggers of the counter indicate the minimum position.

The number of the signal inversions occurring in the amplifier 6 and the circuits 7 and 8, should be combined with the connection of the binary-numerical converter 7 to the triggers of the counter 3 in such a manner that an excess of pulses appearing at the output of the gate circuits brings about the tendency to close the gate 2 by means of the control voltage coming from the amplifier 6.

The pulses appearing at the output are taken off at the terminal 10.

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WHAT WE CLAIM IS:—

1. A generator for producing a quasi random series of pulses which can have only two values, the number of pulses having one of said values being a desired fraction of the number of pulses generated by the pulse generator, comprising a periodic pulse generator, a gate circuit, at the output of which the pulses of only one of said values can appear, an input for the periodically generated pulses, a combined input for a noise voltage and a control voltage, which modifies the threshold level of said gate input, said control voltage being obtained by counting the pulses appearing at the output of the gate circuit in a counter, and diminishing the counter number by a fraction of the pulses generated by the pulse generator, said fraction representing the desired probability of occurrence of a pulse at the output of the gate circuit, and further by converting the contents of the counter into a numerical signal from which said control voltage, which slowly fluctuates with respect to the repetition frequency of the generator, is derived by means of suitable filters.

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2. A generator as claimed in claim 1, wherein the counter counts in normal binary code, and is provided with a binary-numerical converter which converts only the most significant digits of the contents of the counter to a numerical signal.

3. A generator for producing a quasi random series of pulses which can have only two values substantially as described with reference to the accompanying drawing.

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COMPLETE SPECIFICATION

1 SHEET

*This drawing is a reproduction of
the Original on a reduced scale.*

