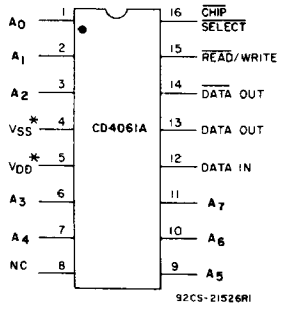
COS/MOS 256-Word by 1-Bit Static Random-Access Memory

Features:

- Low standby power: 10 nW/bit (typ.) @ V_{DD} = 10 V
- Access time: 380 ns (max.) @ V_{DD} = 10 V
- Single 3-to-15 V power supply
- COS/MOS input/output logic compatibility
- TTL output drive capability
- Three-state data outputs for bus-oriented systems
- 1101-type pin designations*
- Separate data output and data input lines
- Noise immunity: 45% of V_{DD} (typ.)
- Fully decoded addressing
- Single write/read control line



The RCA-CD4061A is a single monolithic integrated circuit containing a 256-word by 1-bit fully static, random-access, NDRO memory. The memory is fully decoded and requires 8 address input lines (A_0-A_7) to select one of 256 storage locations. Additional connections are provided for a READ/WRITE command CHIP SELECT DATA IN, and DATA OUT and DATA OUT lines.

To perform READ and WRITE operations the CHIP-SELECT signal must be low. When the CHIP-SELECT signal is high, read and write operations are inhibited and the output is a high impedance. To change addresses, the CHIP-SELECT signal must be returned to a high level, regardless of the logic level of the READ/WRITE input. In a multiple package application, the CHIP-SELECT signal may be used to permit the selection of individual packages.

Output-voltage levels appear on the outputs only when the CHIP SELECT and READ/WRITE signals are both low. Separate data inputs and outputs are provided; they may be tied together, or, to eliminate interaction between READ and WRITE functions, may be used separately. The circuit arrangement permits the outputs from many arrays to be tied to a common bus.

All input and output lines are buffered. The CD4061A output buffers are capable of direct interfacing with TTL devices.

The CD4061A is available in a hermetically sealed 16-lead dual-in-line ceramic package (CD4061AD) or in chip form (CD4061AH).

MAXIMUM RATINGS,
Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE . . . . . -55 to +125°C

DC SUPPLY-VOLTAGE RANGE:
V_{DD}▲ . . . . . -0.5 to +15 V

DEVICE DISSIPATION (PER PACKAGE) . . . . . 200 mW

ALL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

RECOMMENDED DC SUPPLY VOLTAGE
(V_{DD}-V_{SS}) . . . . . 3 to 15 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

*The pin designations are compatible with other static 256-bit memories and are, therefore, not compatible with standard COS/MOS CD4000A-series devices; i.e., V_{DD} is pin 5 and V_{SS} is pin 4.

CD4061A

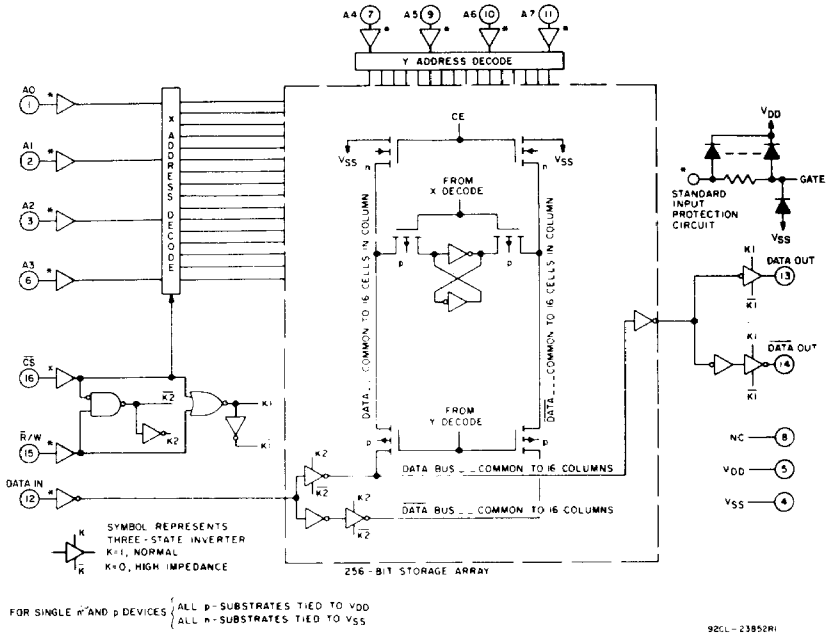


Fig. 1 – CD4061A logic diagram.

CD4061A OPERATIONAL MODES

OPERATION	ADDRESS LINES	CHIP-SELECT	READ/WRITE	DATA IN	DATA OUTPUTS
Write "0"	Stable	0	1	0	High-Impedance
Write "1"	Stable	0	1	1	High-Impedance
Read	Stable	0	0	X	Valid 1 or 0
*Read Modify Write	Stable	0	0/1	X	Valid 1 or 0/High-Impedance
Address Change	Changing	1	X	X	High-Impedance

X = Don't Care

*For a READ MODIFY WRITE operation, CHIP SELECT may be held to logic 0 for the whole operation.

STATIC ELECTRICAL CHARACTERISTICS

(All inputs... $V_{SS} \leq V_I \leq V_{DD}$)

(Recommended DC Supply Voltage ($V_{DD}-V_{SS}$)... 3 to 15 V)

CHARACTERISTIC	TEST CONDITIONS		LIMITS							UNIT
	V_O (V)	V_{DD} (V)	-55°C		25°C			125°C		
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current, I_L *See Fig. 14*		5	–	5	–	0.12	5	–	150	μA
		10	–	10	–	0.25	10	–	300	
Quiescent Device Dissipation/Package, P_D		5	–	–	–	0.6	25	–	750	μW
		10	–	–	–	2.5	100	–	3000	
Output Voltage Low-Level, V_{OL}		5	–	0.01	–	0	0.01	–	0.05	V
		10	–	0.01	–	0	0.01	–	0.05	
High-Level, V_{OH}		5	4.99	–	4.99	5	–	4.95	–	
		10	9.99	–	9.99	10	–	9.95	–	
Noise Immunity, (All Inputs) *See Fig. 17* V_{NL}	0.8	5	1.5	–	1.5	2.25	–	1.4	–	V
	1	10	3	–	3	4.5	–	2.9	–	
V_{NH}	4.2	5	1.4	–	1.5	2.25	–	1.5	–	
	9	10	2.9	–	3	4.5	–	3	–	
Output Drive Current: (Data Out, $\overline{\text{Data Out}}$) N-Channel (Sink), I_DN *See Figs. 3, 4, 12*	0.4	4.5	2	–	1.6	2.5	–	1.1	–	mA
	0.5	10	4.3	–	3.5	5	–	2.4	–	
P-Channel (Source), I_DP *See Figs. 5, 6, 13*	2.5	5	-1.1	–	-0.9	-1.8	–	-0.65	–	
	4.6	5	-0.5	–	-0.4	-0.8	–	-0.3	–	
	9.5	10	-1.1	–	-0.9	-1.8	–	-0.65	–	
Output Off Resistance (High-Impedance State), R_O (Off)		5	10	–	10	–	–	10	–	MΩ
		10	10	–	10	–	–	10	–	

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{SS} = 0 V, C_L = 50 pF, and t_r, t_f = 20 ns

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
		V_{DD} (V)	MIN.*	TYP.	MAX.*	
READ CYCLE TIME						
Read Cycle	t_{RC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	ns
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	ns
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	ns
		10	200	–	–	
Read Access	t_{RA}	5	–	450	750	ns
		10	–	250	380	
Data Out Hold	t_{DOH}	5	110	170	230	ns
		10	130	160	190	
Data Out Active	t_{DOA}	5	80	120	160	ns
		10	40	70	100	
Output Transition	t_{TLH}	5	–	60	100	ns
		10	–	50	75	
	t_{THL}	5	–	35	60	
		10	–	25	40	
Chip-Select Input Rise and Fall Time,	t_{rCE}	5	–	–	15	μs
	t_{fCE}	10	–	–	5	
		15	–	–	1	
WRITE CYCLE TIME						
Write Cycle	t_{WC}	5	1200	1000	–	ns
		10	550	450	–	
Address Setup	t_{ADS}	5	40	0	–	
		10	0	–	–	
$\overline{\text{Chip Select}}$	$t_{\overline{CS}}$	5	700	500	–	
		10	350	250	–	
Address Hold	t_{ADH}	5	460	–	–	
		10	200	–	–	
Write Hold	t_{WRH}	5	150	100	–	
		10	100	70	–	
Write	t_{WRW}	5	150	100	–	
		10	100	70	–	
Data-In Setup	t_{DIS}	5	140	80	–	
		10	80	35	–	
Data-In Hold	t_{DIH}	5	25	10	–	
		10	20	10	–	

* See Symbols Definitions.

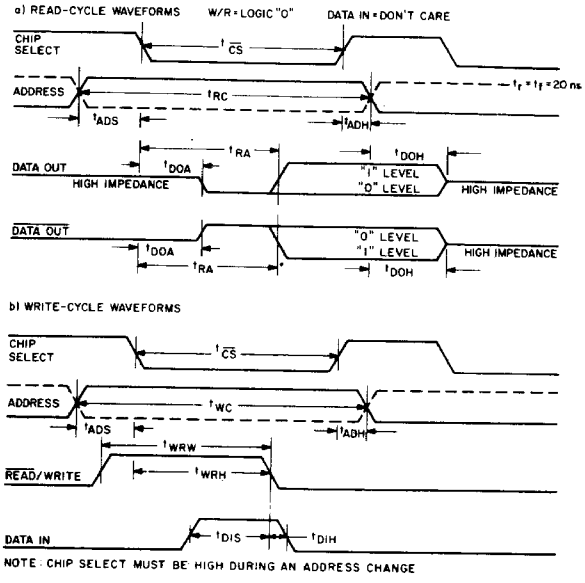


Fig. 2 – Typical write-read waveforms.

SYMBOL DEFINITIONS

t_{RC} – Read Cycle Time – Time required between address changes during a read cycle. Minimum read cycle time is equal to t_{ADS}(min) + $t_{\overline{CS}}$ (min) + t_{ADH}(min).

t_{ADS} – Address Setup Time – Time required before the Chip-Select voltage level can be lowered after the slowest address transition.

t_{ADH} – Address Hold Time – Time required before the earliest address transition can take place after Chip-Select voltage level has been increased. t_{ADH}(min) + t_{ADS}(min) is the minimum time required to discharge internal nodes and allow setting of address decoders during an address transition. Chip-Select level must be high during each address change, even if only read or write cycles are successively performed. However, if address is not changed, the Chip-Select may remain in its active (low) state during successive read and write cycles.

$t_{\overline{CS}}$ – Chip Select Time – Time required for the Chip Select to be active for a valid memory cycle.

t_{RA} – Read Access Time – Measured from Chip Select negative going transition to the valid output data.

t_{DOA} – Data-Out Active – Time required before the high-impedance state of Data Output is changed to a low-voltage state and Data output is changed to a high-voltage state. (If the read out data from a selected storage location is logic "1", then Data Output will rise and Data Output will fall. If the read out data is logic "0", both Data Output and Data Output will maintain their original states.

t_{DOH} – Data-Out Hold – Time required for the Data Output and Data Output to change from an active to a high-impedance state.

t_{WC} – Write Cycle Time – Time required between address changes during a write cycle. This time sets the maximum operating speed for the memory, with a minimum cycle time equal to t_{ADS}(min) + $t_{\overline{CS}}$ (min) + t_{ADH}(min).

t_{WRH} – Write Hold Time – Time required before the negative transition of R/W pulse with respect to the negative transition of the Chip-Select signal.

t_{DIS} – Data-In Setup Time – Time required for the data input to be valid before the negative transition of the R/W pulse.

t_{DIH} – Data-In Hold Time – Time required for the data input to be valid after $\overline{R/W}$ pulse is returned to a low level. The minimum data-in width is equal to $t_{DIS}(min) + t_{DIH}(min)$.

t_{WRW} – Write Width – Time required for the $\overline{R/W}$ pulse to be high. Note that the positive transition of this signal can be made after the $\overline{Chip\text{-}Select}$ signal is high. In addition, the high state of the $\overline{R/W}$ signal shall be within the $\overline{Chip\text{-}Select}$ active state by at least a t_{WRH} period.

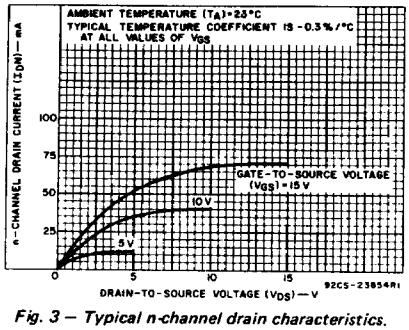


Fig. 3 – Typical n-channel drain characteristics.

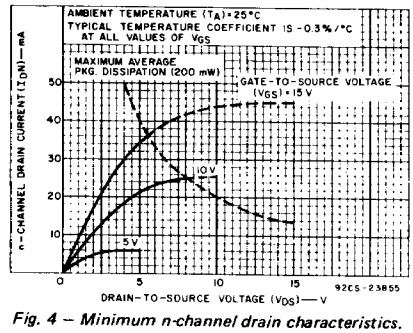


Fig. 4 – Minimum n-channel drain characteristics.

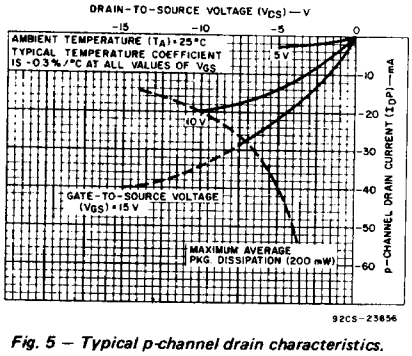


Fig. 5 – Typical p-channel drain characteristics.

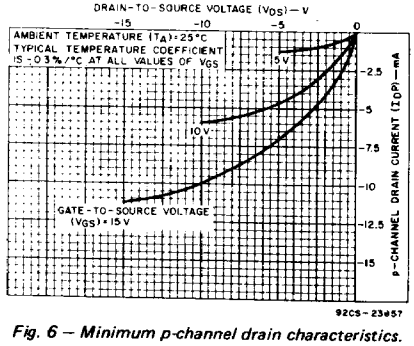


Fig. 6 – Minimum p-channel drain characteristics.

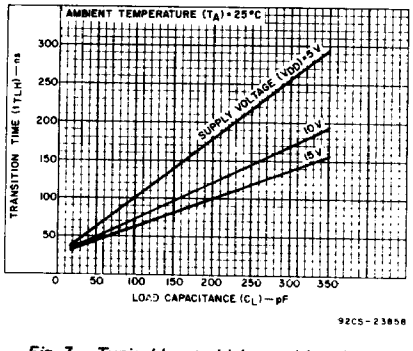


Fig. 7 – Typical low-to-high transition time (t_{TLH}) vs. C_L.

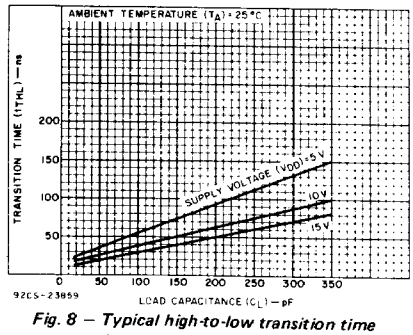


Fig. 8 – Typical high-to-low transition time (t_{THL}) vs. C_L.

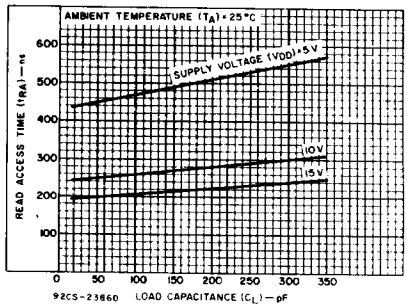


Fig. 9 – Typical read access time (t_{RA}) vs. C_L.

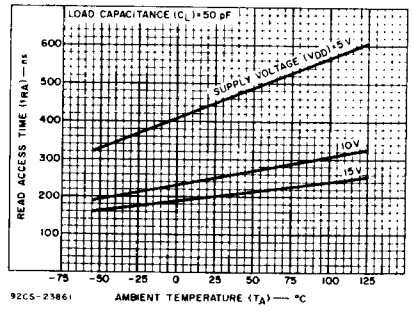


Fig. 10 – Typical read access time (t_{RA}) vs. temperature.

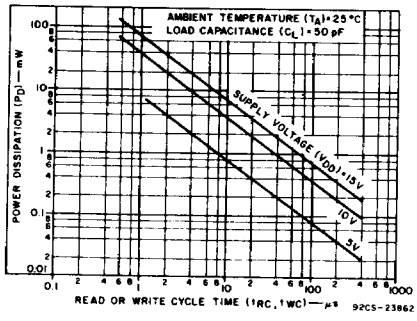
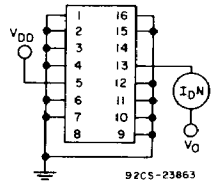


Fig. 11 – Typical power dissipation vs. cycle time.



Note: At address "0", "0" stored in memory.

Fig. 12 – N-channel drive current.

Note for Fig. 12 and Fig. 13:
Power dissipation measured using random data pattern. Input pulse delays and widths set to minimum values specified on data sheet with the exception of cycle time, 15 V setups identical to 10 V data sheet values, with the exception of t_{CE} = 400 ns.

Note: At address 0, "1" stored in memory.

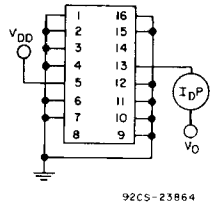


Fig. 13 – P-channel drive current.

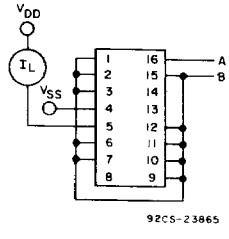


Fig. 14 – Quiescent device current.

Quiescent Device Current Test Conditions

Test	A	B	Memory Cells
1	0	0	All 0
2	1	1	All 0
3	0	1	All 0
4	0	0	All 1
5	1	1	All 1
6	0	1	All 1

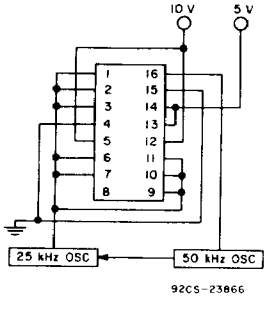
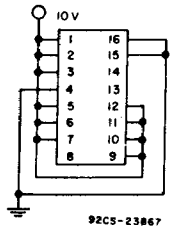


Fig. 15 – Operating life.

Note: Connection to all terminals in Figs. 15 & 16 (except 4 and 5) are made through 47 kΩ resistors.



Description of Test:

Functional test run with random data input. All inputs toggle between 30% and 70% of V_{DD}.

Fig. 16 – Bias life.

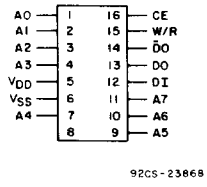
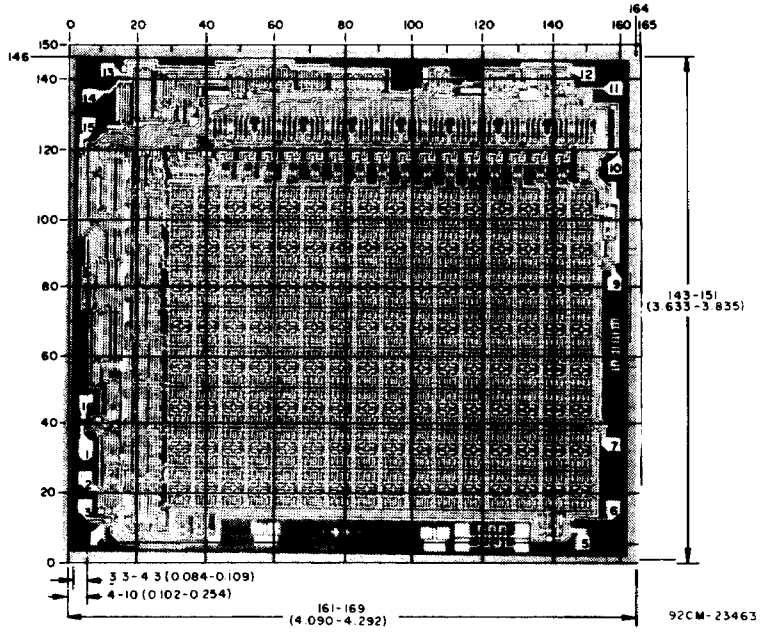


Fig. 17 – Noise immunity.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid Graduations are in Mils (10^{-3} inch).

Dimensions and pad layout for CD4061A.